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Hitachi Microcomputer Technical Q & A H8/300H Series Application Notes



Hitachi Micro Systems, Incorporated 1994

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Introduction

The H8/300H series microcontrollers are high-performance Hitachi-original 16-bit microcontrollers that build in the optimum peripheral equipment for industrial machinery around high-speed H8/300 CPUs that have architecture upwardly compatible with H8/300 CPUs.

The microcontroller puts a CPU, RAM, direct memory access controller (DMAC), bus controller, timers, and a serial communication interface (SCI) on a single chip, making it suitable for a wide range of applications from small to large systems.

This microcontroller technical Q&A covers the H8/3001, H8/3002, H8/3003, H8/3042 series, H8/3032 series, and H8/3048 series.

Table 0-1 H8/300H Series

Item			H8/3003	H8/3002	H8/3001	H8/3042	H8/3041	H8/3040
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	_	_	_	64 k	48 k	32 k
		ZTAT™ *	_	_	_	Yes	_	_
	RAM (b	yte)	512	512	512	2 k	2 k	2 k
Address sp	ace (byte	e)	16 M	16 M	16 M	16 M	16 M	16 M
External da	ata bus w	idth (bit)	8/16	8/16	8/16	8/16	8/16	8/16
Timers	ITU (into	U	5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchd	og timer	1 ch	1 ch	_	1 ch	1 ch	1 ch
DMA	Memory	⁄ ↔ I/O	8 ch	4 ch	_	4 ch	4 ch	4 ch
controller	Memory	√ ↔ memory	4 ch	2 ch	_	2 ch	2 ch	2 ch
Programm controller (ng pattern	16 bits	16 bits	12 bits	16 bits	16 bits	16 bits
SCI (Asyno		clock-	2 ch	2 ch	1 ch	2 ch	2 ch	2 ch
A/D	Resolut	ion	10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
converter	Input ch	annel	8 ch	8 ch	4 ch	8 ch	8 ch	8 ch
	Externa	l trigger input	Yes	Yes	Yes	Yes	Yes	Yes
D/A	Resolut	ion	_	_	_	8 bits	8 bits	8 bits
converter	Input channel		_	_	_	2 ch	2 ch	2 ch
Refresh co	ntroller		On-chip	On-chip	_	On-chip	On-chip	On-chip
Interrupts	Externa	l interrupts	9	7	4	7	7	7
	Internal	Interrupts	34	30	20	30	30	30
I/O port			58	46	32	78	78	78
Package			QFP-112	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100
Miscellane	ous		_	_	_	_	_	_

Note: ZTAT (Zero turn around time) is a trademark of Hitachi Ltd.

Table I-1 H8/300H Series (cont)

ltem			H8/3048	H8/3047	H8/3044	H8/3032	H8/3031	H8/3030
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	128 k	96 k	32 k	64 k	32 k	16 k
		ZTAT™ *	Yes	_	_	Yes	_	_
	RAM (b	yte)	4 k	4 k	2 k	2 k	1 k	512
Address s	pace (byte	e)	16 M	16 M	16 M	1 M	1 M	1 M
External da	ata bus w	idth (bit)	8/16	8/16	8/16	8	8	8
Timers	ITU (into	U	5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchd	og timer	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
DMA	Memory	/ ↔ I/O	4 ch	4 ch	4 ch	_	_	_
controller	Memory ↔ memory		2 ch	2 ch	2 ch	_	_	_
Programm controller (ng pattern	16 bits	16 bits	16 bits	16 bits	16 bits	16 bits
SCI (Asynosynchrono		/clock-	2 ch	2 ch	2 ch	1 ch	1 ch	1 ch
A/D	Resolut	ion	10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
converter	Input ch	annel	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch
	Externa	I trigger input	Yes	Yes	Yes	Yes	Yes	Yes
D/A	Resolut	ion	8 bits	8 bits	8 bits	_	_	_
converter	Input ch	annel	2 ch	2 ch	2 ch	_	_	_
Refresh co	ntroller		On-chip	On-chip	On-chip	_	_	_
Interrupts	Externa	l interrupts	7	7	7	6	6	6
	Internal	Interrupts	30	30	30	21	21	21
/O port			78	78	78	63	63	63
Package			QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-80 TQFP-80	QFP-80 TQFP-80
Miscellaneous				rt card interfaction		_	_	_

For Users of the Microcontroller Technical Q & A

This *Microcontroller Technical Q & A* was compiled from answers to technical questions we received from Hitachi microcontroller users. We hope that it will be a useful addition to the H8/300H series user manuals. Before starting design of products that use microcontrollers, read through the manual to deepen your understanding of microcontroller products and re-familiarize yourself with those areas of difficulty at the design stage.

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Since the CCR's V flag and C flag both flag a 1 when an operation overflows, what is the difference? Registers	pic	The Difference Between	een the CCR's V	Flag and C F	lag		
Answer Answer The CCR's V flag is accessed to see if an overflow has occurred in a signed operation. In figure 1.1, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the negative minimum (H'80) or larger than the maximum (H'7F). Page 1.1 V Flag Operation In contrast, the CCR's C flag is accessed to see if an overflow has occurred in a signed operation. In figure 1.2, which is a byte-sized operation. The flag is set to 1 when the result is smaller than the maximum (H'7F). Pigure 1.1 V Flag Operation In contrast, the CCR's C flag is accessed to see if an overflow has occurred in an unsigned operation. In figure 1.2, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the minimum (H'00) or larger than the maximum (H'FF). Registers Bus controller Interrupts Related Manuals Manual Title Other Technical Document Name Pigure 1.1 V Flag Operation In contrast, the CCR's C flag is accessed to see if an overflow has occurred in an unsigned operation. In figure 1.2, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the minimum (H'00) or larger than the maximum (H'FF). Registers Bus controller Interrupts Resets Power-down mod Instructions Miscellaneous Manual Title Other Technical Document Name Other Technical Document Name Related Microcompute Technical Q&A Title	uestion					С	lassification—H8/300H
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Figure 1.1 V Flag Operation In contrast, the CCR's C flag is accessed to see if an overflow has occurred in an unsigned operation. In figure 1.2, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the minimum (H'00) or larger than the maximum (H'FF). Related Microcomput Technical Q&A Title Overflow				_	-		
In contrast, the CCR's C flag is accessed to see if an overflow has occurred in an unsigned operation. In figure 1.2, which is a byte-sized operation, the flag is set to 1 when the result is smaller than the minimum (H'00) or larger than the maximum (H'FF). C flag		the positive maximum H'80 V flag	n (H'7F).	H'7F	um (H'80) or	Do	cumentation
(H'00) or larger than the maximum (H'FF). Technical Q&A Title Overflow Overflow Overflow Overflow		on the positive maximum V flag Overflow ✓	n (H'7F).	H'7F Overf	um (H'80) or	Do	cumentation
H'00 H'FF C flag	nrger than	on the positive maximum V flag V flag Overflow Figure 1.1 t, the CCR's C flag is a	V Flag Operat	H'7F Overfion	um (H'80) or low v has	Do	cumentation
C flag Overflow ◆ Overflow	n contrast ccurred in	V flag H'80 V flag Figure 1.1 t, the CCR's C flag is a n an unsigned operatio the flag is set to 1 who	V Flag Operat accessed to see in. In figure 1.2, en the result is s	H'7F Overfion if an overflow, which is a b	low v has yte-sized	Do	cumentation cument Name
Overflow ◆ Overflow	n contrast ccurred in	H'80 V flag Overflow Figure 1.1 t, the CCR's C flag is a n an unsigned operation the flag is set to 1 whe larger than the maximus	V Flag Operat accessed to see in. In figure 1.2, en the result is s	H'7F Overfion if an overflow, which is a b maller than t	low v has yte-sized	Dod Dod Rel Tec	cument Name cument Name atted Microcomputer
	n contrast ccurred in	H'80 V flag Overflow Figure 1.1 t, the CCR's C flag is an an unsigned operation the flag is set to 1 who larger than the maximum	V Flag Operat accessed to see in. In figure 1.2, en the result is s	H'7F Overfion if an overflow, which is a b maller than t	low v has yte-sized	Dod Dod Rel Tec	cument Name cument Name atted Microcomputer
E! 1.2 C.El O	n contrast ccurred in	H'80 V flag V fl	V Flag Operat accessed to see in. In figure 1.2, en the result is s	H'7F Overfion of an overflow, which is a boundler than t	low v has yte-sized he minimum	Dod Dod Rel Tec	cument Name cument Name atted Microcomputer
Figure 1.2 C Flag Operation References	n contrast ccurred in	overflow ← H'80 V flag V flag Figure 1.1 t, the CCR's C flag is a n an unsigned operation the flag is set to 1 whe larger than the maximus C flag Overflow ← Creation of the flag is set to 1 when the maximus	V Flag Operat accessed to see in. In figure 1.2, en the result is sum (H'FF).	H'7F Overfion of an overflow, which is a boundler than t	low v has yte-sized he minimum	Dod Dod Rel Tec	cument Name cument Name atted Microcomputer

Product	H8/300H	Q&A No.	QA300H-002A
Topic	The Relationship Between Data Size a	and V Flag C	Changes
Question Do the cha	anges in the CCR's V flag vary with da	ta size?	Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
signed ari However, Byte Word Long	s V flag changes when an overflow is of thmetic operation. This operation is the the timing of the changes in the flag value when the value is smaller than H'80 of the When the value is smaller than H'800 the word: When the value is smaller than H'7FFFFFFF.	same for all aries as follo or larger than 00 or larger t	Il data sizes. ows: n H'7F. than H'7FFF. Other Technical Documentation Document Name
References	5		

Product	H8/300H	Q&A No.	(QA300H-003A
Topic	Use of General Registers			
Question				Classification—H8/300H
G 11.00				Software
	rent general registers be used as 8-bit, 1	6-bit, and 32	2-bit	Registers
registers a	t the same time?			Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
Yes. Regis	sters can be set freely for use as shown E0 R0H	in figure 1.3	3.	Manual Title
	ER1			Other Technical
	E2 R2H	R2L		Documentation
	EZ NZFI	NZL		Document Name
	ER3			See section 2.4.2, General
				Registers, in the following manuals:
	E4 E	4		• H8/3002 Hardware Manual
	E5 E	5		• H8/3003 Hardware Manual
				• H8/3042 Series Hardware
	E6 R6H	R6L		Manual
	ER7 (SP)			Related Microcomputer Technical Q&A
Not	e: ER7 is used as the SP without any spec	cial notice bei	ng given.	Title
	Figure 1.3 Use of General Re	gisters		
References	5		-	
	_			

Product	H8/300H		Q&A No.		QA3	00H-004	
Topic	Bus State While the C	PU Is Operating					
Question					CI	assification	—H8/300H
1 What	t is the bus state during	CDI Lintarnal n	na aasain a?			Software	
1. What	t is the bus state during CPU internal processing?				Registers		
2. What	t is the bus state after $\overline{\overline{D}}$	REQ is received	d?		0	Bus controll	er
			10			Interrupts	
3. What	t is the bus state after \overline{B}	REQ is received	1?			Resets	
						Power-dowr	n mode
						Instructions	
						Miscellaneo	us
						DMA contro	ller
						ITU	
						Watchdog ti	mer
						SCI	
						A/D convert	er
						I/O ports	
_					+_+		
Answer						ated Manual	S
See table	1.1.				Ivian	ual Title	
Table 1.1	Bus State While the C	DII Ia Onovotine	~				
Table 1.1	Dus State Wille the C	I O is Operating	3				
CPU Opera		Address Bus	Data	Bus			
	rnal CPU processing	Hold	High i	mpedance	Oth	er Technical	<u> </u>
After DREC	s received	DMA address	DMA			umentation	
After BREC	is received	High impedance	e High i	mpedance	Doc	ument Nam	е
					Rele		External Bus the following
						uals: 8/3002 <i>Hard</i> v	vare Manual
						8/3003 Hardv	
						8/3042 Series	Hardware
					M	anual	
						ated Microco nnical Q&A	omputer
					Title	•	
References	S						
ı							

Product	H8/300H	Q&A No.	. QA300H-005A		
Topic	Bus Modes				
Question				Classification—H8/300H	
Section 6	2.1 of the H8/3003 Hardware Manual s	ave "When	even 1 hit	Software	
	WCR is cleared to 0, the bus mode bec	-		Registers	
	all areas can be accessed in 16-bit mod		s. Does tins	Bus controller	
incuir that	an areas can be accessed in 10 bit moc			Interrupts	
				Resets	
				Power-down mode	
				Instructions	
				Miscellaneous	
				DMA controller	
				ITU	
				Watchdog timer	
				SCI	
				A/D converter	
				I/O ports	
Answer				Related Manuals	
bit is clear might bett the H8/30 used as the	(bus width control register) is cleared to red can be accessed in 16-bit mode. The rer read, "When even one area is set as 0H CPU goes into 16-bit bus mode and e data bus. This means that I/O ports the bus (D7–D0) cannot be used as generate."	e manual de a 16-bit acco l D15–D0 ca at are also u	scription essed space, an all be used as the	Other Technical Documentation Document Name See table 6.4, Address Space and Data Bus Used, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual • H8/3042 Series Hardware	
				Manual Related Microcomputer	
				Technical Q&A	
				Title	
References	5				

Product	H8/300H	Q&A No.		QA3	300H-006A
Topic	Setting the Bus Controller in Area 7				
Question				С	lassification—H8/300H
a:	7		1.1		Software
	7 mixes on-chip RAM and internal I/O				Registers
areas are t	he bus widths and access states set by t	ne dus conti	roner vana?		Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
controller registers.	the bus width and number of access state are valid in areas other than the on-ch (The addresses of the area differ accord for details.) On-chip RAM has a fixed number of access states of 2. The integral of the control of the contro	ip RAM and ding to the p	l internal I/O product. See of 16-bits	Ма	nual Title
controller registers. the manua and a fixed have bus v	are valid in areas other than the on-ch (The addresses of the area differ accord of for details.) On-chip RAM has a fixed d number of access states of 2. The interviolation of 8-bits or 16-bits, and have a f	ip RAM and ding to the pd bus width ernal I/O reg	l internal I/O product. See of 16-bits jisters can	Oth	nual Title ner Technical cumentation
controller registers. the manua and a fixe	are valid in areas other than the on-ch (The addresses of the area differ accord of for details.) On-chip RAM has a fixed d number of access states of 2. The interviolation of 8-bits or 16-bits, and have a f	ip RAM and ding to the pd bus width ernal I/O reg	l internal I/O product. See of 16-bits jisters can	Oth Do	ner Technical
controller registers. the manua and a fixed have bus v	are valid in areas other than the on-ch (The addresses of the area differ accord of for details.) On-chip RAM has a fixed d number of access states of 2. The interviolation of 8-bits or 16-bits, and have a f	ip RAM and ding to the pd bus width ernal I/O reg	l internal I/O product. See of 16-bits jisters can	Oth Do Do See Ma in t • H • H	ner Technical cumentation cument Name e figure 6.2, Access Area p for Each Operating Mode, he following manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual
controller registers. the manua and a fixed have bus v	are valid in areas other than the on-ch (The addresses of the area differ accord of for details.) On-chip RAM has a fixed d number of access states of 2. The interviolation of 8-bits or 16-bits, and have a f	ip RAM and ding to the pd bus width ernal I/O reg	l internal I/O product. See of 16-bits jisters can	Oth Do Do See Ma in t • H • H M	ner Technical cumentation cument Name e figure 6.2, Access Area p for Each Operating Mode, he following manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware
controller registers. the manua and a fixed have bus v	are valid in areas other than the on-ch (The addresses of the area differ accord for details.) On-chip RAM has a fixed number of access states of 2. The interviolets of 8-bits or 16-bits, and have a fixed that it is a fixed to the control of the	ip RAM and ding to the pd bus width ernal I/O reg	l internal I/O product. See of 16-bits jisters can	Oth Do Do See Ma in t • H • H M	ner Technical cument Name e figure 6.2, Access Area p for Each Operating Mode, he following manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual lated Microcomputer chnical Q&A

When the RAME (RAM enable) bit of the SYSCR (system control register) is cleared to 0, the on-chip RAM is not valid and the settings of area 7 are followed. The CS signal outputs low in all of area 7.

Product	H8/300H	Q&A No.		QA:	300H-007A
Topic	External Installation of RAM to 8-Bit Bi	us Areas			
Question				(Classification—H8/300H
XXII DA	M	1 . 1			Software
when KA	M is externally installed in 8-bit bus spused to access it, \overline{HWR} or \overline{LWR} ?	ace, which s	agnal		Registers
should be	used to access it, HWK of LWK?			0	Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
II 41 II	W/D - ' 1			Ma	nual Title
Use the H	WR signal.				
					her Technical cumentation
				Do	cument Name
				Se	e table 6.4, Address Space
					d Data Bus Used, in the
					lowing manuals: H8/3002 Hardware Manual
					H8/3002 Hardware Manual
					H8/3042 Series Hardware
				1	Manual
				Re Te	lated Microcomputer chnical Q&A
				Tit	le
References	8				

Product		H8/300H	Q&A No.	QA300H-008A-1				
Topic		Changing the Number of Wait States I	Changing the Number of Wait States Inserted Per Area					
Question 1. Can 2. If no		he wait mode be set for individual areas, how should the wait mode be set to c s states inserted for individual areas?	as?			Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports		
2.	WMS regist reaso The f	S (wait mode select) bits 1 and 0 of the ter), which set the wait mode, are common, the wait mode cannot be set for individual areas, can, however, be mixed wait disabled areas. Areas to which wait states are only insequence of wait mode 0) Areas in which WC (wait count) bits 1 availed (programmable wait mode, pin wait mode) number of access states for individual are these in combination. An example is second in the	non to all are vidual areas. d: erted by the and 0 of the ait mode 1, or	WAIT pin WCR are or pin auto-	Oth Do Do See Set foll • H • H M Rei	nual Title ner Technical cumentation cument Name e section 6.3.5 (5), WSC ting Example, in the owing manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual lated Microcomputer chnical Q&A		

References

The bus width and the enabled/disabled state of WSC (wait state controller) operation can be set for individual areas.

Product	H8/300H	Q&A No.	QA300H-008A-2				
Topic	Changing the Number of Wait States Inserted Per Area						
Answer							

Example: To set the following access states for the following areas:

Areas 0-1: 2 states
Area 2: 3 states
Areas 3-4: 4 states
Area 5: 5 states
Areas 6-7: 6 states

Table 1.2 Changing the Number of Wait States Inserted Per Area

Area	Memory Map	Wait States from WC Bit	Enable/Disable of Wait Insertion from WAIT Pin	Waits from WAIT pin	Access States
Area 0	2-state access space	Invalid	Disable	_	2
Area 1	Wait-disabled area				
Area 2	3-state access space pin wait mode 0	Invalid	Enable	0	3
Area 3		Valid/1 state	Enable	0	4
Area 4	3-state access space pin wait mode 1				
Area 5			Enable	1	5
Area 6	3-state access space	Invalid	Enable	3	6
Area 7	pin wait mode 0				

Table 1.3 Register Settings

Register	Address	Setting
		7 0
ASTCR (Access state control register)	H'FC	1 1 1 1 1 0 0
		7 0
WCER (Wait state control enable register)	H'38	0 0 1 1 1 0 0 0
		7 0
WCR	H'F9	

Prod	luct	H8/300H	Q&A No.		QA	300H-009A
Topic	С	Receiving BREQ in Power-Down Mod	е			
Ques	stion				C	Classification—H8/300H
						Software
1.	Can l	BREQ be received in sleep mode?				Registers
2.	Can Ī	BREQ be received in hardware/softwar	e ctandhy m	ode?		Bus controller
۷.	Cann	SKEQ be received in nardware/softwar	c standby in	ouc:	\vdash	Interrupts
						Resets
						Power-down mode
						Instructions
						Miscellaneous
						DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
Ansv	ver				_	lated Manuals
1.	Yes				Ма	inual Title
2.		e both the hardware standby mode and software standby mode				
		on-chip peripheral modules to a halt (i	ncluding the	e clock),		
	BRE	Q cannot be received.				
						her Technical cumentation
					-	cument Name
					D0	cument Name
					Re	lated Microcomputer chnical Q&A
					Tit	
Refe	rences	•				
IVEIC	Terroes	•				

Product	H8/300H	Q&A No.		QA:	300H-010A	
Topic	Maximum Wait Time After BREQ Input	t				
Question					Classification—H8/300H	
			_		Software	
Why does	it take so long between \overline{BREQ} input an	nd BACK oi	ıtput?		Registers	
					Bus controller	
					Interrupts	
					Resets	
					Power-down mode	
					Instructions	
					Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
					SCI	
					A/D converter	
					I/O ports	
					" o porto	
Answer				Re	lated Manuals	
				Ma	nual Title	
Because th	ne BREQ request is held in the following	ng cases:				
	n DMAC (DMA controller) data is being or block transfer mode.	ng transferre	d in burst			
	n waits are inserted during accesses of				her Technical cumentation	
Example:	When an instruction with a word-size			Document Name		
	with an 8-bit bus in pin wait mode 1:					
	inserted wait states + wait states insert	ted by pin) >	< 2.			
				Re	lated Microcomputer	
				Te	chnical Q&A	
				Tit	le	
References						

Product	H8/300H	Q&A No.	QA300H-011A
Topic	Interrupt Sampling		
Question			Classification—H8/300H
	J		Software
When are	external interrupts (NMI, IRQn) sample	led?	Registers
			Bus controller
			Interrupts
			Resets
			Power-down mode
			Instructions
			Miscellaneous
			DMA controller
			ITU
			Watchdog timer
			SCI
			A/D converter
			I/O ports
Answer			Related Manuals
			Other Technical Document Name See figure 18.17, Interrupt Input Timing, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual See figure 20.17, Interrupt Input Timing, in the following manual: • H8/3042 Hardware Manual Related Microcomputer Technical Q&A
References	S		Title

Prod	luct	H8/300H	Q&A No.		QA3	00H-012A	
Торі	С	Holding External Interrupts					
Que	stion				С	lassification—H8/300H	
1.	Arat	the IRQn interrupt requests held if they are produced when the			Software		
1.		in the IRQII interrupt requests held if they at (IRQ enable) bit of the IER (IRQ en	_			Registers	
	_	ols external interrupts (IRQn), is cleared	-), which		Bus controller	
	Conti	ois externar interrupts (irtQii), is cleare	a to o.		0	Interrupts	
2.	Are I	RQn interrupt requests held if they are	produced w	hen		Resets	
		rupts are masked with the I and UI bits	of the CCR	(condition		Power-down mode	
	code	register)?				Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
						A/D converter	
						I/O ports	
Ansv	ver				Rel	ated Manuals	
1.	1. Yes. When the signal specified by the ISCR (IRQ sense control register) drives the IRQn pin, the IRQnF (IRQn flag) of the ISR (IRQ status register) is set to 1. This is not affected by the state of the IRQnE bit. When the IRQnE bit is set to 1 while the IRQnF is set to 1, an interrupt is requested. The IRQnF bit can be cleared with						
	softw	vare.			_	er Technical cumentation	
2.		As in the above case, IRQnF is not affe	-		Dog	cument Name	
		UI bits. When the IRQnE and IRQnF bits are set to 1 and the				figure 5.2, IRQ Interrupt	
	interi	pt mask is cleared, the interrupt is accepted.		Block Diagram, in the following manuals: • H8/3002 Hardware Manual			
						8/3003 Hardware Manual	
						8/3042 Series Hardware	
					M	lanual	
		1	ated Microcomputer hnical Q&A				
					Title	е	
Refe	rences	8			1		

Product	H8/300H	Q&A No.		QAS	800H-013A	
Topic	Receiving NMIs During NMI Processing	ng	1			
Question				C	Classification—H8/300H	
TC 1 ND 4					Software	
	I has the highest priority and is always				Registers	
routine is	ccepted if it is generated while the NM	rocessing		Bus controller		
Toutille is	running?				Interrupts	
					Resets	
					Power-down mode	
					Instructions	
					Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
					SCI	
					A/D converter	
					I/O ports	
Answer				Re	lated Manuals	
running, t	hat interrupt request is accepted supering	nposed over	the first.			
				Other Technical Documentation		
				Do	cument Name	
				Re	lated Microcomputer	
				Tec	chnical Q&A	
				Tit	le	
References	•					
THOUSE STREET						

Product	H8/300H	Q&A No.		QAS	300H-014A	
Topic	Edge Rise and Fall Times for Interrupt	Pins				
Question				С	Classification—H8/300H	
****					Software	
	edge trigger is used for an external inte	rrupt, what a	are the		Registers	
longest an	lowed rise and fall times of the edge?			Bus controller		
					Interrupts	
					Resets	
					Power-down mode	
					Instructions	
					Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
					SCI	
					A/D converter	
					I/O ports	
A						
Answer				Related Manuals		
Make it no effects:	o more than 2 states. More than this wil	ll produce th	e following	IVIA	nual Title	
1. Interdetec	rupts will not be accepted because the ϵ ted.	edge change	is not			
	than one edge will be detected interna			Other Technical Documentation Document Name		
the e	xternal pin signal, so multiple interrupt	s will be req	uested.			
					lated Microcomputer chnical Q&A	
				Titl	le	
	I					
References	5					

				Г			
Product		H8/300H	Q&A No.		QA300H-015A		
Topic	C	Disable Timing for Interrupts					
Ques	stion				Cla	assification—H8/300H	
						Software	
1.		nterrupts disabled the instant that the personal to the personal to the control of the control o	eripheral mo	odule's		Registers	
	interi	upt enable bit is cleared to 0?	upt enable bit is cleared to 0?				
2.	When	n the interrupt enable bit of the IER (IR	Q enable re	gister) is		Interrupts	
		ed to 0, are interrupt instantly disabled?	-	,		Resets	
						Power-down mode	
						Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
						A/D converter	
						I/O ports	
Ansv	ver				Rela	nted Manuals	
1.	Inter	rupts are disabled after the instruction t	hat cleared t	he interrupt	Man	ual Title	
		e bit to 0 finishes executing. When an		_			
		rated while the zeroing instruction is ex		•			
	reque	est is accepted after the instruction com	pletes its ex	ecution.		er Technical umentation	
2	T4		1 4 . 1 1 4	1		ument Name	
2.		rupts are disabled after the instruction to bit to 0 finishes executing. When an		_		section 5.5.1, Interrupt	
		ated while the zeroing instruction is ex		•		eration and Disable	
	_	est is not accepted after the instruction of	-	_		tention, in the following	
		the request signal is cleared simultaneous			manı	uals: 8/3002 Hardware Manual	
		lowever, since the IRQn flag is held, th	-			8/3002 Hardware Manual	
		e bit is set to 1, that interrupt is accepte		•	• H8	8/3042 Series Hardware	
					Mo	anual	
					Rela Tech	ated Microcomputer	
					Title		
					Also	see section 1.3.2,	
						ling External Interrupts	
					(QA	300H-012A), in this manual.	
Refe	rences	3					

Product	H8/300H	Q&A No.	(QA30	0H-016A
Topic	Exception Processing After a Reset				
Question				Cla	assification—H8/300H
					Software
Are interr	Are interrupts ever generated immediately following resets?				Registers
					Bus controller
				0	Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rela	ted Manuals
	diately after a reset, all interrupts, inclu However, when the first instruction of a accepted.			Doc	er Technical umentation ument Name
				After manu • H8 • H8 • H8	section 4.2.3, Interrupts a Reset, in the following tals: 1/3002 Hardware Manual 1/3003 Hardware Manual 1/3042 Series Hardware 1/3041 Mardware
					ted Microcomputer nnical Q&A
				Title	
References	5		,		

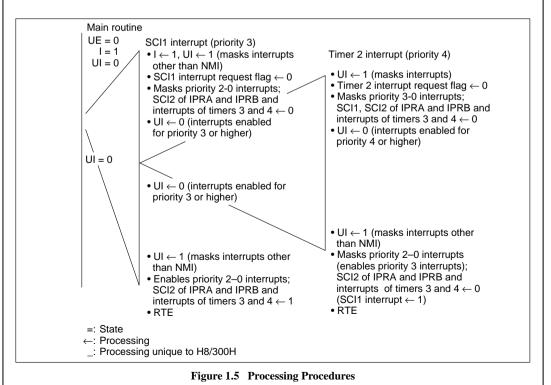
Product	H8/300H	Q&A No.	C	QA300H-017A-1
Торіс	Using the Interrupt Controller			
Question				Classification—H8/300H
** 1		1. 1	66 .:	Software
	ald the two interrupt priority levels be u	sed to make	effective	Registers
use of the	interrupt controller?			Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
			-	Watchdog timer
				SCI
			_	A/D converter
				I/O ports
			-	70 ports
			_	
Anguar				Related Manuals
Answer			-	Manual Title
A and B) be change easy to ma	ing the values set in IPRA and IPRB (in for every interrupt processing routine, to d at any time. IPRA and IPRB are 1-we anipulate. A sample program is shown a fitter the figure for a more concrete ex	he interrupt ord registers in figure 1.4	priority can , so they are . See the	
•				Other Technical Documentation
P	USH R0 — Saves cont	ent of R0		Document Name
M	IOV.W @IPRA, R0 — Saves IPRA	A value		
	USH R0 [→]	IDD A		
	OV.W #NEW, R0 Sets the ne	w IPRA value	to NEVV	
	NDC #H'BF, CCR ——— Clears the	JI bit		
	E : E : E : E : E : E : E : E : E : E :	he sayed IDB	A value	Related Microcomputer
	IOV.W R0, @IPRA	ilie saveu IFR	A value	Technical Q&A
	OP R0 — Reverts to	he saved R0	value	Title
R	TE			
	Figure 1.4 Sample Progra	m		
Reference	S			

Product	H8/300H	Q&A No.	QA300H-017A-2
Topic	Using the Interrupt Controller		
Answer			

- 1. Procedure for setting interrupt priority:
 - a. Set the UE (user bit enable) bit of the SYSCR (system control register) to 0, the I bit (interrupt mask) of the CCR (condition code register) to 1, and the CCR's UI (user bit/interrupt mask) bit to 0. In this state, only NMIs and priority 1 interrupt sources are accepted.
 - b. Set the interrupt priorities for each interrupt source on the user end.
 - c. Perform the following processing during the interrupt processing routines. Following the interrupt priorities set by the user, interrupts of priorities lower than the interrupt in question are masked by writing a 0 to the appropriate bits in IPRA and IPRB.
- 2. Figure 1.5 shows the processing procedures when the interrupt priorities set by the user are as shown in table 1.4.

Table 1.4 Interrupt Priorities

Interrupt Source	User-Set Priorities		Initial IPRA, IPRB Settings
Timer 1	5	Highest	1
Timer 2	4	A	1
SCI 1	3		1
Timer 3	2		1
Timer 4	1	*	1
SCI 2	0	Lowest	1



Product	H8/300H	Q&A No.		QA300H-018A		
Topic	Receiving an External IRQ1 After Retu	ırning From I	Hardware Standby Mode			
hardware	dware standby mode, I set the IRQ1 pir standby mode. Will interrupts be acceppin remains low?			Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports		
hardware and IRQ1 0). Therea	will not be accepted immediately after standby mode. This initializes the IER becomes disabled (the IRQ1E (IRQ1 eafter, if the IRQ1E bit of the IER is set to the standard of the IER is set to the standard of the IER will be a	(IRQ enable nable) bit of the contract of the	e register) f the IER =	Related Manuals Manual Title Other Technical Documentation Document Name See section 4.2.3, Interrupts After a Reset, in the following manuals: • H8/3002 Hardware Manual • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A Title		

Product	H8/300H	Q&A No.		QA3	800H-019A
Topic	Interrupt Priority Within Groups				
Question				С	Classification—H8/300H
					Software
	en external interrupts occur simultaneou				Registers
the	same priority (for example, IRQ4–IRQ7) which has	priority?		Bus controller
2. Wh	en an IRQ4 interrupt occurs during an I	RO7 interrur	ot processing		Interrupts
	tine, what happens? (Does IRQ4 wait or				Resets
tak	e priority?)				Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
2. The mast the pro in t	riority is set within the IRQ4–IRQ7 inte 25 > IRQ6 > IRQ7. IRQ7 is accepted first. After it is accepted. When the I (interrupt mask) and UCCR (condition code register) are enable cessing routine, IRQ4–IRQ7 can be accepted IRQ7 processing routine, the IRQ4 is in the IRQ7 processing routine.	ted, IRQ4–II I (interrupt red during the	RQ7 are all mask) bits of e IRQ7 not enabled	Oth Do Do See Add Ran • H • H • M Rei	ner Technical cumentation cument Name table 5.3, Interrupt Factors, Vector lresses, and Interrupt Priority king (1), in the following manuals: 18/3002 Hardware Manual 18/3042 Series Hardware Manual lated Microcomputer chnical Q&A

Product	H8/300H	Q&A No.	QA3	00H-020A
Topic	Interrupts When the Bus Is Released			
Question			С	lassification—H8/300H
A		111.10		Software
Are interr	upts that occur when the bus is released	i neid?		Registers
				Bus controller
			0	Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
				, с роло
Answer			Rel	ated Manuals
	After the bus release ends, they are acc truction. This is the same regardless of r level.		Ma	nual Title
				er Technical cumentation
			Do	cument Name
				ated Microcomputer hnical Q&A
			Titl	е
References	5			

Product	H8/300H	Q&A No.	Q	A300H-021A
Topic	NMI Sampling Timing and Receiving A	After Reset		
After rese	t, when does sampling of the NMI sign	al begin?		Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
system clo accepted,	of the NMI signal begins simultaneous ock in which the reset clear was sample however, until after the execution of the scleared (see figure 1.6)	rall of the is not ction after	Related Manuals Manual Title Other Technical occumentation	
φ RES	t _{RESS} t _{RESS} sam	et clear pling NMI samp	F	Related Microcomputer Sechnical Q&A
Fig References	gure 1.6 NMI Sampling Timing and Rec	eiving After	Reset	

Product	H8/300H	Q&A No.		QA300H-022A	
Topic	Initializing SP After Reset				
Question				Classification—	H8/300H
	I			Software	
	the SP (stack pointer) have to be initia	lized immed	liately after	Registers	
a reset?				Bus controller	
				Interrupts	
				○ Resets	
				Power-down r	node
				Instructions	
				Miscellaneous	
				DMA controlle	
				ITU	
				Watchdog time	er
				SCI	
				A/D converter	
				I/O ports	
Answer				Related Manuals	
processing address, to them corre	PC (program counter) is saved by the ing becomes undefined. The PC could be to the I/O registers and so on, which makes on the I/O registers and so on, which makes on the I/O registers and so on, which makes on return. This can cause run-awalize the SP immediately after a reset.	written to a kes it impos	blank sible to read	Other Technical Document Name See section 4.2.3, In After a Reset, in the manuals: • H8/3002 Hardwa. • H8/3003 Hardwa. • H8/3042 Series Hanual Related Microcom Technical Q&A Title	e following re Manual re Manual lardware
1					

Product	H8/300H	Q&A No.		QA300H-023A
Topic	Pin State During Power-On Reset			
Question				Classification—H8/300H
XX71				Software
wnat pin	states do I need to pay attention to duri	ng power-or	resets?	Registers
				Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
				·
Answer				Related Manuals
	pins (MD0–MD2) and keep the \overline{STBY} that the ϕ output data is undefined unt			Other Technical Documentation
				Document Name
				See section 3.1.1, Types of Operating Mode Selection, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual • H8/3042 Series Hardware Manual
				Related Microcomputer Technical Q&A
				Title
References	S			

Product	H8/300H	Q&A No.	(QA300H-024A
Topic	RESO Pin Output From RES Pin Input	t		
Question				Classification—H8/300H
				Software
What is th	the \overline{RESO} pin state for reset state (\overline{RES} =	= low)?		Registers
				Bus controller
				Interrupts
				Resets
			-	Power-down mode
				Instructions
			_	Miscellaneous
				DMA controller
			-	ITU
				Watchdog timer
			_	SCI
			_	
			_	A/D converter
			-	I/O ports
			_	
Answer			_	Related Manuals Manual Title
go to reser	t output ($\overline{\text{RESO}} = \text{low}$).		_	Other Technical Documentation Document Name
				Related Microcomputer Technical Q&A
				Title
References	S		l	

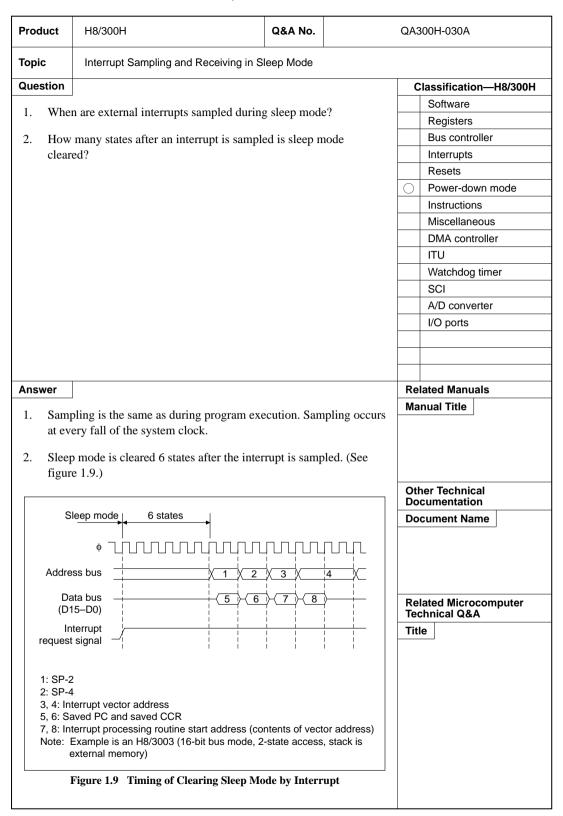
Product	H8/300H	Q&A No.		QA300H-025A
Торіс	Connecting RES and RESO Pins			
Question				Classification—H8/300H
T. (1	PESO dia la constitue de la co			Software
	y problem with taking RESO pin low of the RES pin?	output and ii	iputting it	Registers
directly to	the RES pin?			Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
at that mo initialized the RES in cannot be point cannot	ctly to the \overline{RES} pin, a reset caused by \overline{R} ment and everything internal to the LS. This forcibly disables the \overline{RESO} output spec t_{RESW} (\overline{RES} pin pulse width) satisfied and the operation of the H8/30 to be guaranteed. A buffer thus needs to \overline{ESO} output does not find its way to the	I, including ut as well, m minimum of the country after the country and the co	the WDT, is neaning that of 10 t _{cyc} ter that d to ensure	Other Technical Documentation Document Name
Periph	RES RESO H8/300H		External	Related Microcomputer Technical Q&A
References	Figure 1.7 Connecting RES and R	EESO Pins		

Are there any cautions for reset input? Register: Bus cont Interrupt: Resets Power-de Instruction Miscellar DMA cor	
Are there any cautions for reset input? Registers Bus cont Interrupt Resets Power-de Instructio Miscellar DMA cor)
Are there any cautions for reset input? Registers Bus cont Interrupt Resets Power-de Instructio Miscellar DMA cor	
Registers Bus cont Interrupts Resets Power-de Instructio Miscellar DMA cor	S
Interrupt: Resets Power-de Instructio Miscellar DMA cor	
Resets Power-di Instructio Miscellar DMA cor	roller
Power-de Instruction Miscellar DMA cor	S
Instruction Miscellar DMA corr	
Miscellar DMA cor	own mode
DMA cor	ons
	neous
	ntroller
ITU	
Watchdo	g timer
SCI	
A/D conv	verter
I/O ports	
Answer Related Man	uals
When the RES pin is made low, a reset begins, but to be sure that a reset is performed, it must be low for at least 20 ms when the power is turned on and at least 10 system clock cycles when operating. When it goes high thereafter, reset exception processing begins. If these conditions are not satisfied, operation thereafter cannot be guaranteed.	
Other Techni Documentati	
Document N	ame
See section 4.	
Sequence, in t	he following
manuals: • H8/3002 Ha	ırdware Manual
	ırdware Manual
	ries Hardware
Manual	
Related Micr Technical Q8	
Title	
References	

Topic Executing Instructions When Switching to Hardware Standby Mode Classification—H8/300H Software Registers Bus controller Interrupts Resets Dower-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports	Product	H8/300H	Q&A No.		QA30	0H-027A
What happens to executing instructions when the \$\overline{STBY}\$ pin goes low and the hardware standby mode is entered? Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports A/D converter I/O ports CRAM enable) bit of the SYSCR (system control register) to 0. Related Manuals Manual Title Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: H8/3002 Hardware Manual H8/3042 Series Hardware Manual Related Microcomputer Tu Watchdog timer SCI A/D converter I/O ports Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: H8/3002 Hardware Manual H8/3004 Series Hardware Manual H8/3042 Series Hardware Manual Related Microcomputer Tu Watchdog timer SCI A/D converter I/O ports Watchdog timer SCI A/D converter I/O	Topic	Executing Instructions When Switching	g to Hardware	e Standby Mode	е	
Answer Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Answer Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: - IR83002 Hardware Manual - IR83002 Hardware Manual - IR83002 Hardware Manual - IR83002 Hardware Manual - IR83004 Series Hardware Manual Related Microcomputer Technical Q&A Related Microcomputer Technical Q&A	Question				Cla	ssification—H8/300H
and the hardware standby mode is entered? Registers	*****		CEPY :	,		Software
Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Manual • H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A Related Microcomputer Technical Q&A			STBY pin g	goes low		Registers
Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Related Manuals Manual Title Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: H8/3002 Hardware Manual See section 19.3.1, Transition to Hardware Standby Mode, in the following manuals: H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A	and the ma	irdware standby mode is entered?				Bus controller
Answer Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Related Manuals Manual Title Related Manuals Manual Title Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A Related Microcomputer Technical Q&A						Interrupts
Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3002 Hardware Manual Related Microcomputer Technical Q&A						Resets
Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Related Manuals Manual Title Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manuals: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: - H8/3003 Hardware Manual					0	Power-down mode
Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • #8/3002 Hardware Manual • #8/3003 Hardware Manual • #8/3042 Series Hardware Manual Related Microcomputer Technical Q&A						
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Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A					\vdash	
Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: - #8/3002 Hardware Manual - #8/3003 Hardware Manual - #8/3042 Series Hardware Manual - #8/3042 Series Hardware Manual - #8/3042 Series Hardware Manual Related Microcomputer Technical Q&A					-	
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Answer The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Documentation Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual • H8/3042 Series Hardware Manual • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A						
The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A						I/O ports
The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A						
The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A						
The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0. Other Technical Document Name See section 17.5.1, Transition to Hardware Standby Mode, in the following manuals: • H8/3002 Hardware Manual See section 19.5.1, Transition to Hardware Standby Mode, in the following manual: • H8/3042 Series Hardware Manual Related Microcomputer Technical Q&A	Δnswer				Rela	ted Manuals
	cannot be	guaranteed. To preserve the contents o	f RAM, clea	r the RAME	See s to Ha the fo H8. See s to Ha the fo H8. See s to Ha the fo H8. Ma	ection 17.5.1, Transition ardware Standby Mode, in billowing manuals: /3002 Hardware Manual /3003 Hardware Manual ection 19.5.1, Transition ardware Standby Mode, in billowing manual: /3042 Series Hardware mual ted Microcomputer inical Q&A

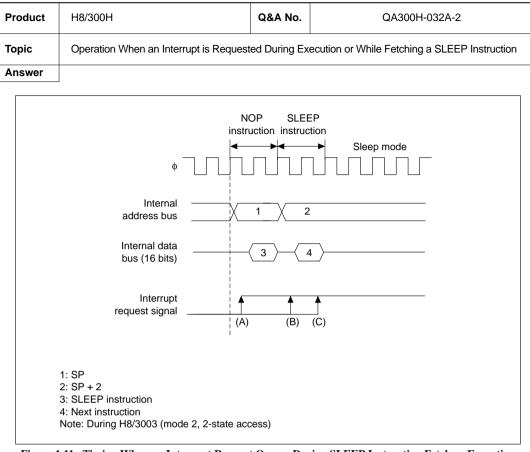
Product	H8/300H	Q&A No.		QA	300H-028A
Topic	Mode Pins During Hardware Standby	Mode			
Question				C	Classification—H8/300H
XX71 . 1	1 4 1 1 (4/D2 14/D2)	1	1 .		Software
	pens when the mode pins (MD2–MD0)	are change	1 in		Registers
nardware	standby mode?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
the mode	is abnormal hardware standby mode of pins while in hardware standby mode. O PROM mode, for example, the power	When the m	ode is		
					her Technical cumentation
				Do	cument Name
				Po	loted Microcomputer
					lated Microcomputer chnical Q&A
				Tit	le
References	3				

Product	H8/300H	Q&A No.		QA300H-029A
Торіс	Returning From Hardware Standby Mo	ode		
high to ret	at the RES pin has to be kept low and the turn from hardware standby mode, but it is changed to high does the RES pin h	how long be	fore the	Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
100 ns bei	from hardware standby mode, the RES Fore the STBY pin is changed to high. (Related Manuals Manual Title Other Technical Documentation Document Name See Appendix E, Hardware Standby Mode Transition (Return Timing), in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual • H8/3042 Series Hardware
References	Figure 1.8 Standby Release T	iming		Manual Related Microcomputer Technical Q&A Title



Product	H8/300H	Q&A No.		QA3	00H-031A
Topic	Execution Time in Software Standby N	Mode	1		
Question				С	lassification—H8/300H
**		C.			Software
	y states are needed to transition to the s	software star	idby mode		Registers
using a Si	LEEP instruction?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					, о ром
Answer				Rel	ated Manuals
	J			Ма	nual Title
	required to transition to the software sta	-			
	quired for the SLEEP instruction to exc				
	n is stated in on-chip memory, it takes 2				
	struction is in external 8-bit 3-state-acce figure below shows the timing for except the state of the state o	_			
	n. (See figure 1.10.)	ecution of th	e SLEEF	Oth	ner Technical
ilisu ucuoi	ii. (See figure 1.10.)				cumentation
	SLEEP			Do	cument Name
	instruction				
	execution time)			
	 ← →	Sleep mode			
			-	Rel	ated Microcomputer
	Internal \(\frac{1}{2} \)		.		chnical Q&A
	address bus 1 2		-	Titl	е
	Internal data		.		
	bus (16 bits) 3 4				
	1 1 1				
1: PC					
2: PC+					
	EEP instruction tt instruction (not executed)				
	Figure 1.10 Sleep Instruction	Timina			
	rigure 1.10 Steep Instruction	ımıng			
Ī				1	

Product	H8/300H	Q&A No.		QA300H-032A-1	
Горіс	Operation When an Interrupt is F	Requested During Exe	ecution or While	e Fetching a SLEEP Instruc	tion
Question				Classification—H8/3	300H
How door	the U9/200U CDU energte who	n an interment acma	e in durina	Software	
	the H8/300H CPU operate whe nstruction fetch or while a SLE			Registers	
a SEEEL 1	instruction reten or white a SEE	El mistraction is ca	ccuting:	Bus controller	
				Interrupts	
				Resets	
				O Power-down mode	3
				Instructions	
				Miscellaneous	
				DMA controller	
				ITU	
				Watchdog timer	
				SCI	
				A/D converter	
				I/O ports	
				'	
nswer				Related Manuals	
				Manual Title	
shown bel A. Durin	ng SLEEP instruction fetch: The	interrupt exception	n processing		
	after the previous instruction fi				
	mes the address of the SLEEP in		-	Other Technical Documentation	
the in	terrupt service routine, the SLE	EP instruction exec	eutes.	Document Name	
B. Durir	ng SLEEP instruction execution	(case 1): Interrupt (exception	Document Name	
	essing starts without going throu	•	_		
_	ecomes the address of the instru				
instru	action. After returning from the	interrupt service ro	utine, the		
	action after the SLEEP instruction	_		Delete d Misses ensemble	
				Related Microcompute Technical Q&A	er
	£ , , , ,			Title	
	eled 6 states later and the interru	pt service routine s	tarts. (See		
ngur	e 1.11.)				
References	*				
COLOR CHICES	<u>.</u>				



Figure~1.11~Timing~When~an~Interrupt~Request~Occurs~During~SLEEP~Instruction~Fetch~or~Execution

Produ	ıct	H8/300H	Q&A No.		QA300H-033A
Topic		Support for the DAA (DAS) Instruction	with the INC	(DEC) Instruc	ction
1. 2.	The I but h	DAA instruction can be used with an acow about executing it after an INC inst DAS instruction can be used with a subow about executing it after an DEC ins	ruction exec tract instruc	cutes?	Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
	Execuinstruthe reincre with Execuinstruthe redecre with	ution of a DAA instruction after executation is not supported, since the C and esults of the operation after INC instruction decimal data, execute a DAA institute ADD instruction (ADD.B #1, Rd). ution of a DAS instruction after executation is not supported, since the C and esults of the operation after DEC instruction decimal data, execute a DAS institute ADD instruction (ADD.B #-1, Rd H flags (XORC #A0, CCR).	H flags do a etion execution afte ion of an DI H flags do a ction execut cruction afte	not reflect fron. To r adding 1 EC not reflect cion. To r adding –1	Related Manuals Manual Title Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title
Actu		eration is determined by the flag state.			

Prod	luct	H8/300H	Q&A No.		QA:	300H-034A	
Topi	С	BRA and BRN Instructions					
Ques	stion				(Classification—H8/300H	
1	33.71	's the difference between DDA (DT)	1 DADO A1			Software	
1.		is the difference between BRA (BT) a it mean for the condition to be "True"?	so, wnat		Registers		
	does	it mean for the condition to be True ?			Bus controller		
2.	What	does it mean for the BRN (BF) condit	ion to be "Fa	alse"?		Interrupts	
						Resets	
						Power-down mode	
						Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
						A/D converter	
						I/O ports	
						<u> </u>	
Ansv	ver				Re	lated Manuals	
					Ma	nual Title	
1.		BRA instruction can be used just like th	ne JMP instr	uction, but			
		rs in the following points:	120	1 1. O			
		It can only branch in the range +127 by		bytes for d:8			
		and +32767 bytes to -32768 bytes for our of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not one of the relative values of objects do not object on the relative values of objects do not object on the relative values of objects do not object on the relative values of objects do not object of the relative values of objects do not object on the relative values of objects do not object of the relative values of objects do not object of the relative values of objects do not object of the relative values of objects do not object of the relative values of of the		rogram can			
		be relocated.	mange, me j	orogram can	Ot	her Technical	
		Execution states and instruction size ar	e different.		Documentation		
		Assembler format is different.	0 01110101111		Do	cument Name	
		ndition of True means that since this in		vays			
	branc	thes, the branch condition is always Tru	ie.				
2.	2. A condition of False means that since this instruction never						
		thes, the branch condition is always Fal		,,,,		lated Microcomputer	
						chnical Q&A	
					Tit	ie	
Pofo	rences						
Keie	ences						

		H8/300H					300H-035A	
Горіс	1	BRN Instruction						
Questio	n					С	lassificati	on—H8/300
What ki	ind of	instruction is BRN (BI	E)3				Software	
w nat Ki	iliu Ol	illistruction is DKIV (DI	1.);				Registers	3
							Bus conti	roller
							Interrupts	3
							Resets	
							Power-do	own mode
						0	Instructio	
							Miscellan	
							DMA con	troller
							ITU	
							Watchdo	g timer
							SCI	
							A/D conv	
							I/O ports	
BRN is		evenient instruction that				_	lated Manu	uals
BRN is instruct instruct 1.5.	ions o	during debugging. It open out its size and execution	erates the sai	me as the NO	OP	Ма	nual Title	
BRN is instruct instruct 1.5.	ions o	during debugging. It open out its size and execution The BRN Instruction	erates the san	me as the NO as described	OP I in table	Ma		cal
BRN is instruct instruct 1.5.	ions o	during debugging. It open out its size and execution	erates the san	me as the NO as described	OP	Ma Otil Do	nual Title	cal on
BRN is instruct instruct 1.5. Table 1.	ions o	during debugging. It open out its size and execution The BRN Instruction	erates the san	me as the NO as described	OP I in table	Ma Otil Do	nual Title her Techni cumentati	cal on
BRN is instruct instruct 1.5. Table 1. Instruct	ions of ion, b	during debugging. It open but its size and execution The BRN Instruction Instruction Size (Bytes)	erates the san n time differ	me as the NO as described	OP I in table	Ma Otil Do	nual Title her Techni cumentati	cal on
instruct instruct 1.5. Table 1. Instruct	ions dion, b	during debugging. It operate its size and execution The BRN Instruction Instruction Size (Bytes)	erates the san n time differ) Instructio	me as the NO as described	OP I in table	Ma Otil Do	nual Title her Techni cumentati	cal on
BRN is instruct 1.5. Table 1. Instruct NOP Note:	ions of ion, b	during debugging. It operate its size and execution The BRN Instruction Instruction Size (Bytes) 4 2 16-bit bus/2-state access s	n time differ Instruction 4* 6* 2*	me as the NC as described	OP I in table Time (States)	Otil Do	nual Title her Techni cumentati cument Na	cal on ame
BRN is instruct 1.5. Table 1. Instruct NOP Note:	ions of ion, b	during debugging. It operate its size and execution The BRN Instruction Instruction Size (Bytes) 4 2 16-bit bus/2-state access s	n time differ Instruction 4* 6* 2*	me as the NC as described	OP I in table Time (States)	Otil Do	nual Title her Techni cumentati cument Na	cal on ame

Product	H8/300H	Q&A No.		QAS	300H-036A
Topic	The SUBX Instruction				
Question				C	Classification—H8/300H
***** 1			.1 7		Software
	the SUBX instruction (subtraction with	h carry) pres	serve the Z		Registers
mag when	the result of execution is 0?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					1
Answer				Re	lated Manuals
multiple s reflects the	X instruction is used to divide a subtract ubtractions. After the SUBX instruction e result of all of these operations (See for results of each individual SUBX instru	n is executed figure 1.12.)	d, the Z flag		
	— SUB R	mL, RnL			ner Technical cumentation
	Reflected in Z flag ◀	,		Do	cument Name
	_	RmH, RnH			
	Figure 1.12 Z Flag				
When the	SUBX instruction results in a 0, the Z	flag thus ho	ds the result		
	vious operation.	inag unas no	ids the result		lated Microcomputer chnical Q&A
				Tit	le
References	8				

Product	H8/300H	Q&A No.	(QA3	300H-037A			
Topic	Odd Address Values During STC Instr	Odd Address Values During STC Instruction Execution						
Question				С	lassification—H8/300H			
****	and a second				Software			
	e odd address value when an STC instr		ecuted and		Registers			
the CCR s	tored in an (register indirect) even add	ress?			Bus controller			
					Interrupts			
				\Box	Resets			
					Power-down mode			
				0	Instructions			
				Ť	Miscellaneous			
					DMA controller			
				\neg	ITU			
					Watchdog timer			
			-		SCI			
					A/D converter			
			-		I/O ports			
			-		"о роло			
			-					
			-					
Answer				Rei	ated Manuals			
Undefined			-		nual Title			
				Doc	ner Technical cumentation cument Name lated Microcomputer chnical Q&A			
D-1-								
References	5_							

Prod	luct	H8/300H	Q&A No.		QA:	300H-038A
Торі	С	Interrupts and DMA Transfer Requests	While the E	EPMOV Instruc	ction	Is Executing
Que	stion				(Classification—H8/300H
1.	Who	on interrupt occurs during the executi	on of an EE	DMOV		Software
1.		n an interrupt occurs during the executing an interrupt resection, what happens to that interrupt re		PIVIOV		Registers
	msut	iction, what happens to that interrupt re	quest:			Bus controller
2.		happens when a DMA transfer reques	t occurs dur	ing the		Interrupts
	execu	ition of an EEPMOV instruction?				Resets
						Power-down mode
					0	Instructions
						Miscellaneous
						DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
Ans	wer				_	lated Manuals Inual Title
2.	finish occur occur the by opera	action, the interrupt is held and accepted these executing. It is handled the same as as during ordinary instruction execution are during EEPMOV.W execution are accepted in transfer is completed. For interruption is the same as for EEPMOV.B. DMA transfer is executed between the of the EEPMOV instruction.	when an int a. However, tepted after that pts other that	errupt NMIs that transfer of an NMIs,	Do Do Sec 2), ma • H	her Technical cumentation cument Name e section 2.2.28 (items 1 and EEPMOV, in the following nual: 18/300H Series Programming Manual clated Microcomputer chnical Q&A
Refe	rences	3				

Product	H8/300H	Q&A No.		QA3	00H-039A
Topic	The Difference Between EEPMOV.B a	nd EEPMOV	′.W		
Question				С	lassification—H8/300H
What is th	ne difference between EEPMOV.B and	EEPMOV.W	7?		Software
			-		Registers
					Bus controller
					Interrupts
			_		Resets
					Power-down mode
			_	0	Instructions
			_		Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	ated Manuals
Size EEPI EEPIEnab EEPI EEPI	of register that counts the transfer bytes MOV.B: Byte (maximum number of tra MOV.W: Word (maximum number of tra MOV.W: Word (maximum number of tra MOV.B: Accepted after instruction execution (all of the MOV.W: NMI alone is accepted after transleted (all others held).	s: nsfer bytes ransfer bytes cutes (all he	is 255). s is 65535).	Door See EED + H	ner Technical cumentation cument Name section 2.2.28 (1), (2) PMOV 18/300H Series trogramming Manual lated Microcomputer
References	S				

Product	H8/300H	Q&A No.		QA	300H-040A
Topic	Cautions on Stack Operation				
Question				(Classification—H8/300H
A 41	, 				Software
Are there	any particular cautions about stack ope	ration to be	aware or?		Registers
					Bus controller
					Interrupts
					Resets
				Power-down mode	
					Instructions
				0	Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
When the Use the P	8/300H, the stack area is always accessed stack pointer is set to an odd number, rush or POP instructions to stack. The sundefined. It is initialized by the user.	nalfunctions	can result.	Do See Res For • H • H • M	her Technical cumentation cument Name section 2.4.4 Inicial CPU sistor, section 2.5.2 Memory Data mats, in the following manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual lated Microcomputer chnical Q&A
References	S				

Product	H8/300H	Q&A No.		QA3	300H-041A		
Торіс	On-Chip Peripheral LSI Access When	the Bus Is R	eleased				
Question				С	lassificatio	n—H	8/300H
					Software		
	nal devices (bus master) access internal				Registers		
device?	when the H8/300H CPU has released the	ne bus to an	externai		Bus contro	oller	
device?					Interrupts		
					Resets		
					Power-dov	vn mo	ode
					Instruction		
					Miscellane		
					DMA cont		
					ITU		
					Watchdog	timer	,
					SCI		
					A/D conve	rter	
					I/O ports		
Answer				Re	lated Manu	als	
	al registers cannot be accessed from ex				nual Title		
				Do	ner Technic cumentatio cument Na	n	
				Tec	lated Micro	comp	outer
				Titl	16		
References	3			l			

Prod	luct	H8/300H	Q&A No.		QA3	300H-042A
Topi	С	Areas That Can Be Used as ROM by t	he Vector Ta	ble		
Que	stion				С	lassification—H8/300H
,	<u> </u>		1.1			Software
1.		the empty areas of the vector table (reserve) be used as ROM?	erved by sys	tem or		Registers
	reser	ve) be used as ROM?				Bus controller
2.	Can t	the empty areas of the I/O registers be u	ised as RON	1?		Interrupts
						Resets
						Power-down mode
						Instructions
					0	Miscellaneous
						DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
Ansv	ver				Re	lated Manuals
1.	canno	vector numbers reserved by the system of the used. Reserve addresses, however addresses on the vector addresses on the vector.	, can be use	d as ROM.	Ма	nual Title
2.	The e	empty areas of the I/O registers cannot	be used.			ner Technical cumentation
						cument Name
						lated Microcomputer chnical Q&A
					Titl	
Refe	rences	5				

Items reserved by the system are used by development tools. Addresses reserved by the system and reserve addresses are listed in the manual. Branch address areas of "memory indirect" addressing can use addresses other than those reserved by the system or those of used by the vector table.

Product	H8/300H	Q&A No.		QA3	800H-043A
Topic	Pin State During the Oscillation Settlin	g Time			
Question				С	Classification—H8/300H
****					Software
	the pin states during oscillation settling	time after the	he software		Registers
standby m	node is cleared?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
	as in the software standby mode.			_	nual Title
				Do	ner Technical cumentation cument Name
				Tec	lated Microcomputer chnical Q&A
				Tit	le_
References	5				

Product	Common		Q&A No.	QA	300H-101-1
Горіс	Receiving D	MAC Startup Reques	ets		
Question					Classification—H8/300H
W D) 3.6.4				Software
when a D	MA controlle	r startup request occ	urs:		Registers
1. When	n is the reques	t forced to wait?			Bus controller
	1				Interrupts
		oted under the follow	ving conditions?		Resets
		IOV execution			Power-down mode
		nodify-write instruct			Instructions
•	During DMA	C cycle steal transfer	rs.		Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					7 - Реги
nswer				Re	elated Manuals
				, Ma	anual Title
	_		al bus master > refres		
			s that DMA requests		
-			or refresh controller w bus. Since the DMA		
_			03) shown in table 2.1		
	-		annel is transferring.		her Technical
104	ose waits wile	a mgner priority en	umier is trumsterring.	Do	ocumentation
Table 2.1	DMAC Cha	nnel Priority		Do	ocument Name
Short Add	ress Mode	Full Address Mod	le Priority		
Channel 0 Channel 0		Channel 0	Highest Å		
Channel 1 Channel 1		Channel 1			elated Microcomputer
Channel 2 Channel 2		Channel 2			chnical Q&A tle
Channel 3		Channel 3	Lowest		
References	s				

Product	Common	Q&A No.	QA300H-101-2
Topic	Receiving DMAC Startup Requests		
Answer			

2. During EEPMOV execution, requests are accepted between the read cycle and the write cycle. During read-modify-write instruction execution, requests are accepted between the read cycle, instruction fetch, and the write cycle. During cycle steal transfers, requests are accepted if the channel of the transfer request is higher in priority than the current channel.

References

- 1. BSET, BCLR, BNOT, BST and BIST are read-modify-write instructions.
- 2. When the wait is longer than those described above, wait states may have been inserted by a CPU bus cycle that has a DREQ request. (See figure 2.1.)

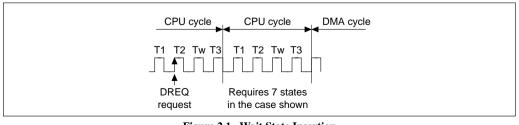


Figure 2.1 Wait State Insertion

Product	Common	Q&A No.		QA	.300H-102
Topic	Addresses During DMA Transfers				
Question				(Classification—H8/300H
D 201	CDI 11 : DMAC		1 4		Software
	ne CPU cause problems in DMAC oper		ads the		Registers
MAK (IIIe	mory address register) during DMA tra	msiers?			Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
However, between r as describ	the MAR does not have any affect on D when longword data is read, a DMA control of the top 16-bits of data and the ed in the manual. As a result, the value value. The timing at which the MAR is	ycle can ento e bottom 16- read may d	er in bits of data, affer from	Ма	nual Title
figure 2.2		1			her Technical cumentation
	, DMA cycle			Do	cument Name
	Td T1 T2 T1	destination			lated Microcomputer chnical Q&A le
2. Count 3. MAR Note: M	updated at transfer source. er updated. updated at transfer destination AR also updated at transfer source at 1' (du the block transfer mode).	ring burst trai	nsfers and		
	Figure 2.2 MAR Update Tin	ning			
References	3				

There should be no mistake in the value read so long as the bottom 16-bit (MARH, MARL) value is read with the MOV.W instruction.

Product	Common	Q&A No.		QA	300H-103
Topic	TEND Signal Output Timing 1				
Question				С	Classification—H8/300H
===					Software
Is the TEN	ND signal output at every byte/word tra	nsfer?			Registers
					Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
(using the the TEND block trans	D signal is output when the startup sour DREQ pin). In operating modes other to signal is driven low during the final transfers, it is low during the write cycle justifier. It is not output at every byte/word.	than block transfer write on the state of th	ansfer mode, cycle. For end of a 1		nual Title
					ner Technical cumentation
	Final DMA cycle	_ CPU cycl	_	-	cument Name
	Td T1 T2 T1 T2 Address bus				ounient runie
	RD			Re	lated Microcomputer
	HWR, LWR	<u> </u> 		Titl	
	TEND				
	Figure 2.3 TEND Outpu	t			
References	S			1	

Product	Common		Q&A No.		Q	A300H-104
Торіс	TEND Sigr	nal Output Timing	2			
Question						Classification—H8/300H
A 4 1 4 4	, t	CENID1	49			Software
At what ti	ming is the I	TEND signal outp	out?			Registers
						Bus controller
						Interrupts
						Resets
						Power-down mode
						Instructions
						Miscellaneous
					C	DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
nswer					R	elated Manuals
	φ	Final DMA	CPU o	ycle		ther Technical ocumentation
	Address bus				D	ocument Name
	RD					
	HWR, LWR					elated Microcomputer echnical Q&A
	TEND					itle
	ETCR	H'01 X	H'00			
	Fig	gure 2.4 TEND (Output Timing			
References	S				ı	

Product	Common		Q&A No.		QA	300H-105	
Торіс	The Relationship Between	en the DMAC's	s DTE and D	TIE Bits			
Question Classification—H8/3					lassification—H8/300H		
When the DTIE (date transfer interment enable) hit is 1 and the DTE (date				a DTE (data		Software	
When the DTIE (data transfer interrupt enable) bit is 1 and the DTE (data transfer enable) bit is then cleared to 0, the manual says that an interrupt				Registers			
is requested of the CPU.					Bus controller		
is requesi	d of the Cr o.					Interrupts	
1. Will	DMA transfer end interru	ipts occur con	tinuously, as	shown in		Resets	
figur	e 2.5?					Power-down mode	
2. If so,	what can be done to kee	p interrupts fro	om occurring	g?		Instructions	
						Miscellaneous	
		DTE = 0, DTIE	= 1			DMA controller	
	DMA interrup					ITU	
	2	. p. c c c c c				Watchdog timer	
		Holds the valu	es			SCI	
		DTE = 0, DTIE	= 1			A/D converter	
						I/O ports	
	(RT	E					
]	Figure 2.5 Continuous In	terrupts from	DTE and DT	ME			
Answer					Re	lated Manuals	
1. Yes,	interrupts will occur cont	impopule			Manual Title		
alwa _y instru	TE = 0 and DTIE = 1 (enarys be produced. To prevenction can be used), or cleation can be used).	nt this, set DT	E to 1 (the I	BSET	Do	ner Technical cumentation cument Name	
			Related Microcomputer Technical Q&A				
					Titl	e	
References	3						

Product	Common	Q&A No.		QA	300H-106	
Topic	DMAC Startup					
Question				C	Classification—H8/300H	
XX71 .1	DMACC: 4 1 14 IMIL	. 1 .			Software	
	DMAC is started up with an ITU comp				Registers	
	ens if the I (interrupt mask) and UI (us	er bu/miem	ipt mask) of		Bus controller	
the CCR (condition code register) are masked?					Interrupts	
					Resets	
					Power-down mode	
					Instructions	
					Miscellaneous	
				0	DMA controller	
					ITU	
					Watchdog timer	
					SCI	
					A/D converter	
					I/O ports	
Answer				Related Manuals		
Interrupts selected as DMAC startup sources are not affected by the					nual Title	
	errupt mask bits (I and UI bits). (See fi		by the			
		B)				
		CVCCD				
		SYSCR				
Per	ipheral module		CR		her Technical cumentation	
Flag		¬→ [ι	ו ווע	_	cument Name	
compa				- 50	cument Name	
the lil		★ ,				
	Interrupt Priority determine the second seco		CPU			
	bit ation	-				
	circuit			Ra	lated Microcomputer	
					chnical Q&A	
			DMAC	Tit	le	
		DT	_			
Figure 2.6 DMAC Startup						
References	<u>.</u>					
iveletetice:	<u>'</u>					

When an interrupt is disabled with an interrupt enable bit in a module, interrupts will not occur for either the DMAC startup request or the CPU.

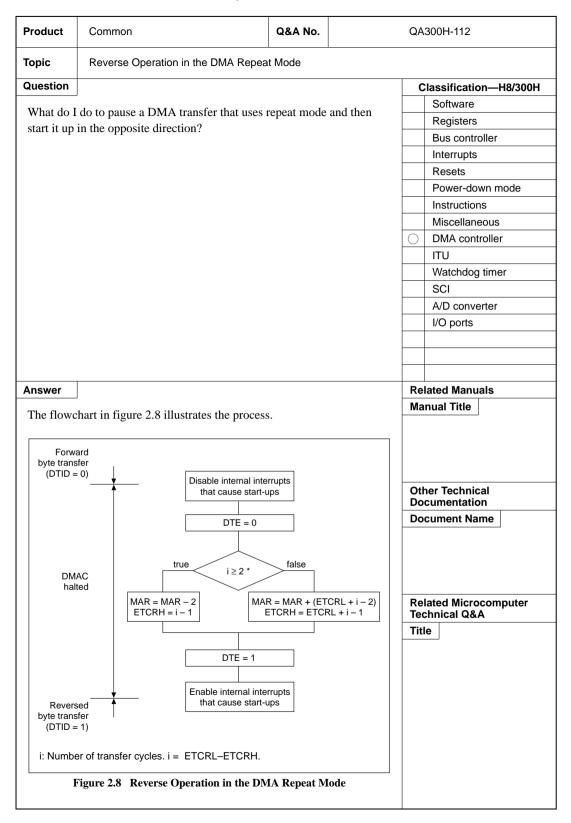
Product	Common	Q&A No.		QA	300H-107
Topic	The DMAC and Timer Interrupts		ı		
Question				С	lassification—H8/300H
					Software
When the DMAC startup source has compare-matched the ITU, is an				Registers	
interrupt p	produced to the CPU of the ITU?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rel	ated Manuals
DTE (data control re When the goes to the	requests selected as startup sources star a transfer enable) bit of the DMAC's D'gister) is set to 1, and no interrupt is generate bit is 0, no startup request is generate an interrupt that is used as a state ously generate an interrupt to the CPU.	TCR (data to nerated to the erated and are artup source	ransfer ne CPU.	Do	ner Technical cumentation cument Name atted Microcomputer chnical Q&A
References	S				

Product	Common	Q&A No.		QA	300H-108
Topic	Operation After a DMAC End Interrupt	Is Generate	d 1		
Question				С	lassification—H8/300H
****					Software
	transfer count register becomes H'0000) while the I	OMAC is in		Registers
use and ar	n end interrupt is generated:				Bus controller
1. When is the next transfer request accepted?					Interrupts
					Resets
	ransfer requests generated before the D	MA transfe	r starts		Power-down mode
ignoi	red?				Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
enab reach of the trans regis 2. Whe reque hard	next transfer request is accepted when the le) bit is set to 1 by software. When the ness H'0000 and a transfer end interrupt is DTCR (data transfer control register) after is disabled. To do another transfer, so the during the end interrupt routine and in the startup request is an internal interested when the DTE bit is 0. For more is ware manual. When the startup request nored if it is an edge.	transfer cousts generated, is cleared and the transfer then set the trupt, a CPU information,	nt register the DTE bit ad data er count DTE bit to 1. interrupt is see the	Do See Use • H • H • M	ner Technical cumentation cument Name section 8.6, Cautions on e, in the following manuals: 18/3002 Hardware Manual 18/3042 Series Hardware Manual 18/3042
Reference	5				

					$\overline{}$	
Product	Common	Q&A No.		QA300H-109		
Topic	Operation After a DMAC End Interrupt Is Generated 2					
Question				Classification—H8/300	Н	
				Software		
	transfer count register becomes H'0000		Registers			
use and th	e transfer ends, when is the transfer en	d interrupt g	enerated?	Bus controller		
				Interrupts		
				Resets		
				Power-down mode		
				Instructions		
				Miscellaneous		
				DMA controller		
				ITU		
				Watchdog timer		
				SCI		
				A/D converter		
				I/O ports		
Answer				Related Manuals		
released. V	ransfer ends, an interrupt request is gen When the CPU captures the bus, the tra lafter the executing instruction ends. (\$\frac{9}{2}\$	nsfer end in	terrupt is	Manual Title		
		pr	xception ocessing tarted by	Other Technical Documentation		
	CPU cycle Final DMA transfer cycle		AC transfer d interrupt	Document Name		
Transi interrupi	fer end t signal			Related Microcomputer Technical Q&A		
	Figure 2.7 Timing at DMAC End	Interrupt	-	Title		
References	s			1		

Product	Common	Q&A No.		QA	300H-110
Topic	DMA Transfers Started up by Serial Tr	ansfers			
Question				С	lassification—H8/300H
C	the mass of the state of the st	1 T	(O1		Software
Can more than 256 transfers be done between memory and I/Os when SCI and DMAC are used together to send and receive?					Registers
SCI and L	DMAC are used together to send and rec	cerve?			Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				Ŭ	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					,, o posso
Answer				Rel	ated Manuals
more data	number of transfers allowed will then than this, data must be stored in memo- set with a transfer end interrupt.			041	an Tashwisel
					ner Technical cumentation
				Do	cument Name
					lated Microcomputer
				Titl	е
References	S			ı	

Product	Common	Q&A No.		QA300H-111
Topic	Time Until DMAC Startup by the DREC	Q Pin		
Question				Classification—H8/300H
				Software
Why is 4 states the minimum time to startup the DMAC from the DREQ				Registers
pin?				Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
	e bus arbiter internal processing time is ninimum of 4 states (the sum of these fi			Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title
References	8			



Product	Common	Q&A No.		QA300H-113		
Торіс	Use of Dual-Function Pins					
Question				Classification—H8/300H		
Will d DMAC: 1 1 d CH : 12: d				Software		
When the DMAC is used under the following conditions, can the $\overline{\text{TEND/CS}}$ dual-function pin be used as a $\overline{\text{CS}}$ output?				Registers		
TEND/CS dual-function pin be used as a CS output?				Bus controller		
Condition	s: Full-address transfer mode, external	request (low	level input	Interrupts		
from DRE	\overline{Q} pin) for the startup source.	_		Resets		
				Power-down mode		
				Instructions		
				Miscellaneous		
				O DMA controller		
				ITU		
				Watchdog timer		
				SCI		
				A/D converter		
				I/O ports		
Answer				Related Manuals		
startup soi	be used as a \overline{CS} output. When external surce, the $\overline{TEND}/\overline{CS}$ dual-function pin caput pin. For more information, see the manual.	oncerned be	comes a	Manual Title		
				Other Technical Documentation		
				Document Name		
				See section 9, I/O Ports, in the		
				following manual: • H8/3003 Hardware Manual		
				Related Microcomputer Technical Q&A		
				Title		
References	3					

Prod	uct	Common	Q&A No.		QA3	300H-114	
Topic	С	I/O Ports and the DREQ Pin					
Question					CI	assification—H8/300H	
						Software	
		w should the DTE (data transfer enable) bit of the DTCR (data				Registers	
		Fer control register) be set to use pins that are used both as			Bus controller		
	DKE	Q pins and I/O ports as I/O ports?				Interrupts	
2.	How	should dual-function pins be set for us	e as DREO	pins?		Resets	
r cristian and r				Power-down mode			
						Instructions	
						Miscellaneous	
					0	DMA controller	
					$\overline{}$	ITU	
						Watchdog timer	
						SCI	
				-		A/D converter	
				-		I/O ports	
				-		1/O ports	
				-			
				-			
Ansv	wor				Pol	ated Manuals	
Allov						nual Title	
1.	They	can be used as I/O ports without regard	d to the DTI	E bit.	IVIGI	idai Title	
2.	Толю	e dual-function pins as DREQ pins, cle	or the DDD	(data			
۷.		tion register) of affected ports to 0. Wh					
		output is detected as $\overline{\text{DREQ}}$ input.	en me ddr	is set to 1,			
	port	output is detected as DREQ input.		-	Other Technical		
					Documentation		
					Document Name		
					Related Microcompute		
				_		hnical Q&A	
					Title	9	
Refe	rences	<u> </u>					
l							

Product	Common	Q&A No.		QA300H-115
Topic	PWM Mode and Interrupts			
Question				Classification—H8/300H
				Software
	ITU is used in the PWM mode and into	_		Registers
	to clear the IMFB (input capture/comp			Bus controller
	er status register) to 0 within the interru B automatically cleared when an IMIE			Interrupts
is the fivil	automatically cleared when all living	interrupt is	generateu:	Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				O ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
The IMEI	Office and to Omithin the in			Manual Title
	If It is a flag must be cleared to 0 within the in the timing when the flag is cleared by the			
figure 2.9		ie program i	S SHOWH III	
figure 2.7	•			
	$\begin{bmatrix} T1 & T2 \end{bmatrix}$	T3		Other Technical
		7	_	Documentation
	Φ			Document Name
A -1 -1	TOD address			
Addre	rss TSR address	\triangle		
	MF			Related Microcomputer Technical Q&A
	*			Title
	\FI	ag cleared		1.00
	Figure 2.9 IMFB Flag			
	3 · · · · · · · · · · · · · · · · · · ·			
References	S			1
Io clear th	ne IMFB flag, use the BCLR instruction	n.		

Product	Common	Q&A No.		QA	300H-116		
Topic	Clearing the Counters						
Question				С	lassificatio	n—H8/300H	
			-		Software		
How do I	clear the ITU counter using software?				Registers		
					Bus contro	ıller	
					Interrupts		
					Resets		_
					Power-dov	vn mode	
					Instruction		
					Miscellane		
					DMA contr		
				0	ITU	0.101	_
					Watchdog	timer	
					SCI		
					A/D conve	rter	
					I/O ports		
					"O porto		_
			-				
Answer				Re	lated Manua	als	
	TCNT (timer counter) by writing H'000 ot cleared by rewriting the TSTR (times			Ма	nual Title		
					ner Technic		
				Do	cument Nar	ne	
					lated Microchnical Q&		
				Titl	le		_
References	8		,				

Product	Common	Q&A No.		QA	300H-117
Торіс	Pulse Output From the ITU				
Question				С	lassification—H8/300H
How do I	get a specific number of pulses output	(cov. 10) one	I than stan		Software
the pulse		(8ay, 10) and	i then stop		Registers
the puise	output:				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
PWN compend: up 1 oper addr	In 1 DMAC channel can be used: Pulses of mode. In this case, the DMAC is start pare match. Set DMA transfers for 10 a nterrupt to stop the ITU. This DMA transfers; set the data transfer so that it draition (transfer data, transfer source address).	nd generate unsfer is aimo oes not affect ress, transfer	a transfer ed at starting et CPU destination	Do	ner Technical cumentation cument Name
TCL (x). Com H8/3	K pin (clock input pin) and events cour When the timer (x) compare register rea pare match interrupt is generated and th 00H, TIOCA0/TCLKC and TIOCB0/T	nted by anoth aches a count te ITU stops. CCLKD are c	ner timer t of 10, a On the lual-		lated Microcomputer
the b	tion pins. For this reason, no extra wiring oard to output pulses from channel 0 and KD as input pins.			Tit	chnical Q&A
	n using software: Generate compare macount with the interrupt processing rout		ts each time		
Reference	S				

Product	Common	Q&A No.		QA	300H-118
Торіс	ITU Cascade Connections				
Question				C	Classification—H8/300H
C.,,	de connections be used with the ITU?				Software
Can casca	de connections de used with the 110?				Registers
					Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
TIOCA0 and TCLE	and PA3 pins of port A are dual function and TIOCB0 of the ITU's channel 0 and XD. This enables direct ITU cascade coviring. The count timing for the ITU in 10.	d clock inpu nnections w	ts TCLKC ithout	Otl	ner Technical
(syste	m clock)			_	cumentation cument Name
I	D/TCLKC D/TCLKD				
	Sar Figure 2.10 ITU Count Tim	mpling ning			lated Microcomputer chnical Q&A
				Tit	le
off the ch	re is no wiring from TIOCA0/TCLKC ip and the load is light, TCLKC and TC match output of TIOCA0 and TIOCB0	CLKD sampl	e the		
References	S			1	

Product	Common	Q&A No.		QA	.300H-119
Topic	Setting the ITU's PWM Output				
Question				С	Classification—H8/300H
					Software
When the ITU is used in PWM mode, how should the TIOR (timer I/O					Registers
control re	gister) be set?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					"O porto
Answer				Re	│ lated Manuals
	I				nual Title
set with the each of the	a setting does not affect PWM output. We pwm bit of the TMDRs (timer mode e channels of the ITU, GRA/GRB are user output setting, regardless of the control	e registers) l used as outp	ocated in ut compare		
					her Technical cumentation
				<u> </u>	cument Name
					lated Microcomputer chnical Q&A
				Titl	
				110	
Reference	S			l	
I					

Product	Common	Q&A No.		QA3	300H-120-1
Горіс	ITU Output and Port Output				
Question				(Classification—H8/300H
When the	ITU is set to toggle output on a GRB (outnut cantu	re/innut		Software
	ual-function register B) compare mate				Registers
_	figure 2.11, what kind of value is output	-	_		Bus controller
	t to ITU output?				Interrupts
					Resets
					Power-down mode
(TCN	Γ value)				Instructions
GRE	·†	ии			Miscellaneous
				_	DMA controller
			/ /		ITU
TIOC	3 output,	<i>v V b</i>	(Time)		Watchdog timer SCI
	output	Y			A/D converter
		, \			I/O ports
	ITU output Port output		ITU output		70 ports
			output or output?		
Set for to	ggle output Set for port output with	: Set for toggle ou			
	compare output upon compare the TIOR match in the TIOR	upon compare match in the TIC		Re	lated Manuals
		er I/O control re		Ma	nual Title
	Figure 2.11 ITU Output and Port	Output (Q)			
					ner Technical cumentation
					cument Name
				Re Te	lated Microcomputer chnical Q&A
				Tit	le
2-6	. I				
References					

Product	Common	Q&A No.	QA300H-120-2
Topic	ITU Output and Port Output		
Answer			

- 1. When port output is changed to ITU output, the value from before the change is output.
- 2. When a compare match signal is generated at the point when the port output is to be changed to ITU output, the value changes. (See figure 2.12.)

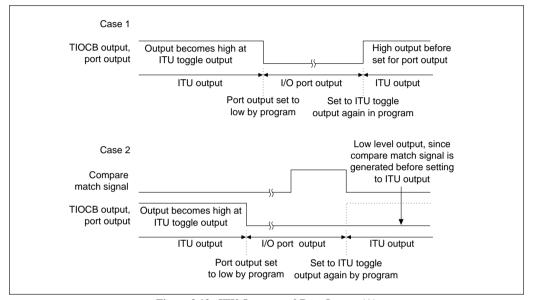
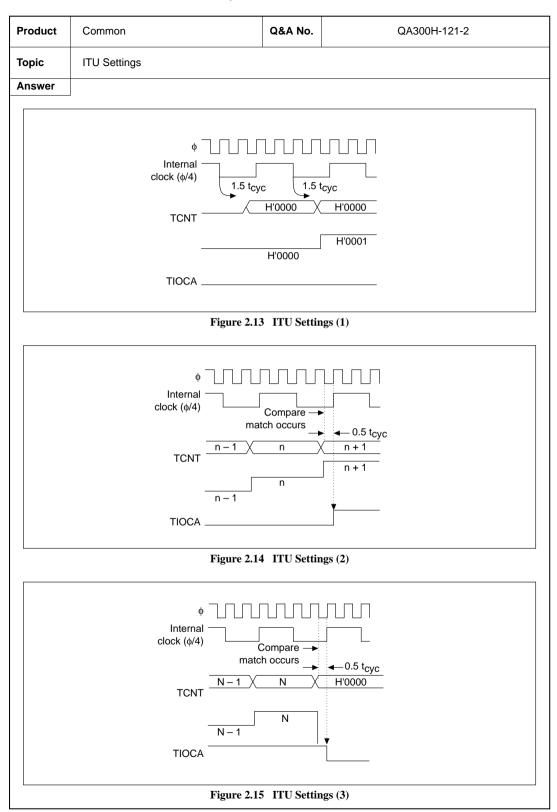


Figure 2.12 ITU Output and Port Output (A)

References

- 1. When the ITU was started after a reset, the TIOCn output is low until the first compare match occurs.
- When set to input capture and output is disabled, the output level changes when an input capture occurs.

Product	Common	Q&A No.		QA300H-121-1
Topic	ITU Settings	•		
Question				Classification—H8/300H
Dlagga avr	aloin in datail the pulse width, evels set	tings and ra	aistar	Software
	plain in detail the pulse width, cycle set or ITU pulse output as well as the relation			Registers
clock.	of 110 pulse output as well as the relativ	onsinp to th	e internar	Bus controller
CIOCK.				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				○ ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
				I/O ports
Answer				Related Manuals
Allswei				Manual Title
the follow	putting pulses in the PWM mode, the dring equation. $= n + 1 / N + 1$			
	e GRA = n (set the counter value corre	sponding to	the Low	
	n-1), and $n-1$ (set the counter value correspondi	ing to the cy	cle _ 1)	Other Technical Documentation
ORD	= 14 (set the counter varie correspondi	ing to the cy	cic – 1)	Document Name
Example:	When the operating frequency is 10 M for the count is $\phi/2$ and GRB = 9, so to (with an N of 9):			
(n +	1)/(9+1) = 0.5			
•	t be set to 4. The exact timing is shown	in figures 2	2.13 to 2.16.	Related Microcomputer Technical Q&A
				Title
References	8			



nswer TCNT value Figure 2.15	Common	Q&A No.	QA300H-121-3
	ITU Settings	,	
TCNT value Figure 2.15			
TCNT value Figure 2.15			
	TCNT value	Figure 2.15	
GRB (N)	GRB (N)		
Figure 2.14	Figur	e 2.14	
		ITU Settings TCNT value	TCNT value Figure 2.15

Figure 2.16 ITU Settings (4)

N

Figure 2.13

TIOCA output Time

Product	Common	Q&A No.		QA	300H-122
Торіс	Independent Operation of TCNT4 Usir	ng Reset-Syr	nchronized PWI	И Мо	de
Question				(Classification—H8/300H
Th	al atotas that "TCNITA many in daman dam	41!!!	4		Software
	al states that "TCNT4 runs independen zed PWM mode is used. Do this mean			Registers	
purposes?		it can be use	d for other		Bus controller
purposes?					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
				\vdash	Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					lated Manuals inual Title
GRB4. Th	ters and registers it uses are TCNT3, G is allows TCNT4 to be used independe o run it as an interval timer using coun	ently. One w	ay to use it		
					her Technical cumentation
				Do	cument Name
					lated Microcomputer
				Tit	
				- 11	
References				•	

Product	Common	Q&A No.		QA	300H-123
Торіс	Halting the WDT's System Clock	ı			
Question				С	lassification—H8/300H
XX 71 .1	The state of the s	 .			Software
when the abnormali	system clock is halted, does the WDT	imer) detect		Registers	
abnorman	ties?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
				0	Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rel	lated Manuals
as well, so	it cannot detect abnormalities.				
					ner Technical cumentation
				Do	cument Name
					ated Microcomputer
					chnical Q&A
				Titl	е
References	S				

Product	Common	Q&A No.		QA	.300H-124
Topic	Using the RDR and TDR When the SC	I Is Not Beir	ng Used		
Question				C	Classification—H8/300H
W/le em 4le e	CCI is not being used.		-		Software
when the	SCI is not being used:				Registers
1. Can	the RDR (receive data register) be used	l as a data re	gister?		Bus controller
					Interrupts
2. Can	the TDR (transmit data register)?				Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				\bigcirc	SCI
					A/D converter
					I/O ports
					-
			-		
Answer				Re	lated Manuals
** 13	•		-	Ма	nual Title
Yes and N	о.				
1. The	RDR cannot be used as a data register b	because it is	a read-only		
regis			,		
2. The	TDR can be used as a data register.				her Technical cumentation
			-		cument Name
			-		
			-	Re	lated Microcomputer
					chnical Q&A
				Tit	le
					<u> </u>
References	3				
	_				

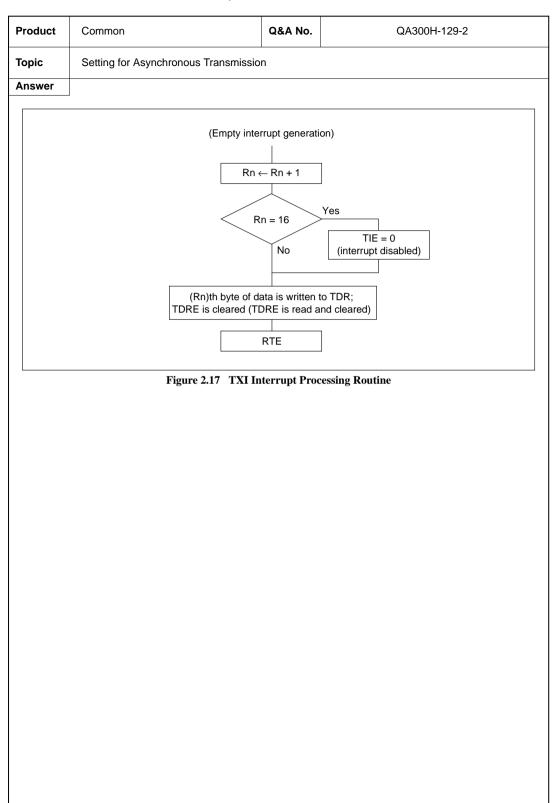
Product	Common	Q&A No.		QA:	300H-125
Topic	I/O Settings of Clock Pins for the SCI				
Question				С	lassification—H8/300H
XX71 .1		1'			Software
	SCI is being used, does the DDR (data				Registers
_	or the SCK (serial clock) pin set the I/O	specification	on for that		Bus controller
pin?					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
A					-1
Answer					ated Manuals nual Title
specified mode regi	irection for the SCK pin when the SCI by the C/\overline{A} bit (communications mode) ster) and the CKE1 and CKE0 (clock entrol register). Setting the DDR of the p	of the SMR nable) bits of	(serial of the SCR		
					ner Technical cumentation
				Do	cument Name
					ated Microcomputer
				Titl	е
References	s				
	_				

Product	Common	Q&A No.		QA	300H-126
Topic	Serial I/O Pin State				
Question				С	lassification—H8/300H
A 64	a the dual function nine that can be use	.d .a. I/O	to (TVD		Software
	g the dual-function pins that can be use				Registers
	SCK) as SCI pins, I reset them as I/O patrol register) and SMR (serial mode register)				Bus controller
	of the DDR (data direction register) pi				Interrupts
the values	of the DDR (data direction register) pr	ns when the	s nappens:		Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
					1/O porto
Answer				Po	lated Manuals
Allowei					nual Title
	tion does not affect the contents of the			IVIC	iluai Title
	as that in the case described above the I	DDR holds t	he value it		
had before	e being set as an SCI pin.				
				041	Took wie ol
					ner Technical cumentation
					cument Name
				Po	lated Microcomputer
					chnical Q&A
				Tit	е
References	S				

Product	Common	Q&A No.		QA	300H-127
Topic	Simultaneous Transmission and Rece	ption with the	e SCI		
Question				С	lassification—H8/300H
XX71 .1					Software
	SCI is being used, can transmission us				Registers
occur sim	ultaneous with reception on the externa	ii clock (or v	ice versa)?		Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
					,, o porto
Answer				Re	lated Manuals
prevents s	ock source can be selected as the SCI tr imultaneous transmission and reception multaneous transmission/reception usin	n using 2 typ	oes of	Ма	nual Title
					ner Technical
					cumentation
				Do	cument Name
					lated Microcomputer chnical Q&A
				Titl	e
			,		
References	5				

Product	Common	Q&A No.		QA	.300H-128
Topic	RDRF				
Question					Classification—H8/300H
					Software
	pens if, when clearing the RDRF (recei				Registers
	R (serial status register) to 0 during SCI	reception, i	t is cleared		Bus controller
to 0 direct	ly without first reading a 1?				Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					-
Answer				Re	lated Manuals
				Ма	nual Title
	be cleared. When the BCLR instruction				
	in byte units, then the bit that correspor 0 and a write occurs, again in byte unit				
	(RXI interrupt processing routine), the				
	ear the RDRF flag.	DCLK IIISU	uction thus		
camot cic	at the KDKI mag.			Ot	her Technical
				Do	cumentation
				Do	cument Name
					lated Microcomputer chnical Q&A
				Tit	
References	S				

Product	Common	Q&A No.		QA300H-129-1
Topic	Setting for Asynchronous Transmission	n		
	nous transmission uses the SCI. How dere (i.e., using the data empty interrupt (Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
the TIE is 1. Settin Rn ← TE = TIE : 2. Settin Rn ← TE = First TDR	TDRE = 1, the data empty interrupt is set to 1. There are thus 2 methods. In the first byte with an interrupt procest of transfer counter) I (transfer enable) I (empty interrupt enable) In the first byte with the initialization: I (transfer counter) I (transfer enable) byte set to TDR E cleared (transfer starts, TDRE = 1 after 1 (empty interrupt enable)	ssing routin	»:	Related Manuals Manual Title Other Technical Documentation Document Name Related Microcomputer Technical Q&A
In either c figure 2.1		ne is as show	n in the	Title



Product	Common	Q&A No.		QA300H-130-1
Topic	How Data Is Transferred to the TDR			
Question				Classification—H8/300H
Are there	wave when transferring transfer data l	ocated in 16	_bit bue	Software
Are there ways, when transferring transfer data located in 16-bit bus space to the SCI's transmit data register (TDR, length 8 bits) as shown in			Registers	
figure 2.13		ingui o oits)	us sno wii iii	Bus controller
				Interrupts
1. Trans	sfer using software?			Resets
2. Use t	the DMAC?			Power-down mode
2. 050 (ine Billine.			Instructions
	\cap			Miscellaneous
	H8/3003			DMA controller
			<u> </u>	ITU
←	SCI	DRAM	1	Watchdog timer
Data tran		Trai	nsfer	O SCI
	DMAC 16-bit	را ا	ata	A/D converter
				I/O ports
	Ų			
	Figure 2.18 Transferring Data to	the TDR		
Answer				Related Manuals
Allower				Manual Title
	t bus spaces can be accessed in byte un			marraur ritio
	e DRAM <u>1 byte at a time</u> and transfer i			
trans	fer data stored in the transfer buffer, do	as shown ii	1 figure 2.19.	
	10000			Other Technical
				Documentation
				Document Name
	10010			
	10010			
No	ote: Start address of transfer buffer 10000	stored in ER0).	Related Microcomputer Technical Q&A
	Figure 2.19 Transfer Buff	er		Title
		-		
D - f				
References	5			

Product	Common			Q&A No.	QA300H-130-2
Topic	How Data Is Transferred to the TDR				
Answer					
LOOP:		#12,R2L for interrupt R2L	Can be p Copy the R3L and	laced in the	
	BNE	LOOP	Continue	e until the tra	ansfer
TxI Interru	pt: MOV.B	@ER0+,R3L	Transfer SCI's TI	the transfer OR	data to the
	MOV.B BCLR BNE	R3L,@TDR #7,@SSR LOOP	Clear TI		counter by 1 ne

2. Using the DMAC: Start up the DMAC with the SCI's TXI interrupt and transfer the transfer data on DRAM 1 byte at a time to the SCI's TDR. Byte needs to be specified as the size in the DMAC. (Word size transfers are impossible, since they start up the DMAC at every transmission of a byte.)

References

The bus controller function can be used to enable word-sized transfers as shown in figure 2.20. For each read cycle (16-bit data), 2 consecutive write cycles of 8-bit data are necessary.

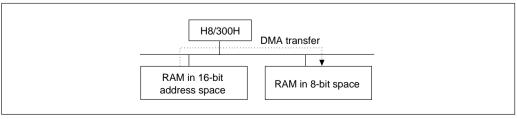


Figure 2.20 Using the Bus Controller Function to Enable Word-Sized Transfers

roduct	Common	Q&A No.		QA30	0H-131A-1
opic	Timing of Setting RDRF				
uestion				С	lassification—H8/300H
When data magnification and a the DDDE (magnification data magnification field) floor					Software
 When data reception ends, the RDRF (receive data register ful of the SSR (serial status register) is set to 1. At what point in t 				Registers	
	hronous mode is the RDRF set?	At what poi	int iii tiic		Bus controller
async	monous mode is the RDR1 set:				Interrupts
2. When	When is it set in clock-synchronous mode?				Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
				Ш	
nswer				Rel	ated Manuals
Basic o	100000000000000000000000000000000000000	5 6 7 8 9 101112	13141516	Do	ner Technical cumentation cument Name
Data sam	pling				
R	DRF -	→			ated Microcomputer hnical Q&A
R	DRF —	→			hnical Q&A
Note: \	DRF When SCK clock source is the internal clock tates. When SCK clock source is an extern			Tec	hnical Q&A
Note: \	When SCK clock source is the internal clock	al clock, 3-4		Tec	hnical Q&A
Note: \	When SCK clock source is the internal clock tates. When SCK clock source is an extern Figure 2.21 8-Bit Data, 1 Stop	al clock, 3-4		Tec	hnical Q&A
Note: \	When SCK clock source is the internal clock tates. When SCK clock source is an extern Figure 2.21 8-Bit Data, 1 Stop	al clock, 3-4		Tec	hnical Q&A
Note: \	When SCK clock source is the internal clock tates. When SCK clock source is an extern Figure 2.21 8-Bit Data, 1 Stop	al clock, 3-4		Tec	hnical Q&A

Product	Common	Q&A No.	QA300H-131A-2
Topic	Timing of Setting RDRF		
Answer			

2. The RDRF flag is set after the MSB data is received and synchronization clock rises. (See figure 2.22.)

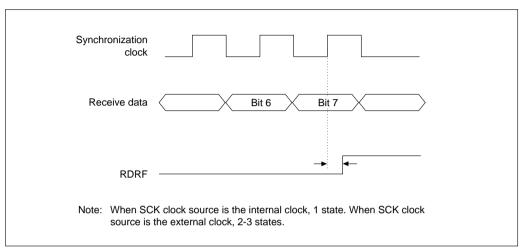


Figure 2.22 8-Bit Data

Product	Common	Q&A No.		QA300H-132A-1		
Topic	Timing of Setting TDRE					
Question				Classification—H8/300H		
			Software			
	en 8-bit data transmission ends, the TDF		-	Registers		
	oty) flag of the SSR (serial status registent in the asynchronous mode is the TDR		At what	Bus controller		
poi	it in the asynchronous mode is the TDR	E set:		Interrupts		
2. Wł	en is it set in clock-synchronous mode?			Resets		
				Power-down mode		
				Instructions		
				Miscellaneous		
				DMA controller		
				ITU		
				Watchdog timer		
				○ SCI		
				A/D converter		
				I/O ports		
Answer				Related Manuals		
the TSR	RE flag is set at different times when the (transmit shift register) and when there enchronous mode. (See figure 2.23.)		ssion data in	Manual Title		
	1 2 3 4 5 6 7 8 9 1011 12131415161 2 3 4 5	5 6 7 8 9 1011 1213	141516	Other Technical Documentation		
Ва	sic clock 1 2 3 4 5 6 7 8 9 10111213141516 1 2 3 4 5			Document Name		
Trans	mit data Stop bit	Start bit				
	TDRE When SCK clock clock, 4 state.	source is the in	ternal	Related Microcomputer Technical Q&A		
	When SCK clock clock, 4–5 state.	source is the ex	rternal	Title		
	CIOCK, 4–5 State.			Title		
	Figure 2.23 Transmit data in TSR (Asynchronous mode)					
Reference	es					

Product	Common	Q&A No.	QA300H-132A-2
Topic	Timing of Setting TDRE		
Answer			

The start of transmission according to the setting of the TE (transmit enable) bit also follows this timing. (See figure 2.24.)

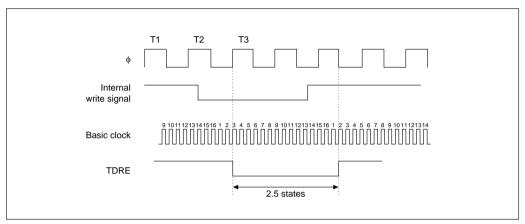


Figure 2.24 No transmit data in TSR (Asynchronous mode)

2. Clock-synchronous mode (See figures 2.25 and 2.26.)

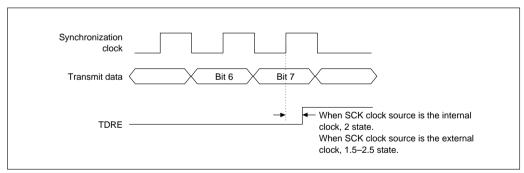


Figure 2.25 Transmit data in TSR (Clock-synchronous mode)

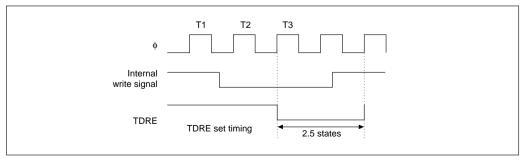


Figure 2.26 No transmit data in TSR (Clock-synchronous mode)

Product	Common	Q&A No.		QA	300H-133
Topic	SCI Reception Errors				
Question					Classification—H8/300H
					Software
	ng to the main routine during a receive				Registers
	earing the reception error flags of the S		tatus		Bus controller
register), i	s a receive error interrupt generated ag	ain?			Interrupts
					Resets
			-		Power-down mode
			-		Instructions
			-		Miscellaneous
			-		DMA controller
					ITU
			-		Watchdog timer
			-	\bigcirc	SCI
			-		A/D converter
			-		I/O ports
			-		1/O ports
			-		
			-		
Answer				Po	lated Manuals
Allowei			-		nual Title
main routi	ve error flag is not automatically cleared ine (after executing the RTE instruction will be generated again.				
					ner Technical cumentation
				Do	cument Name
				Re	lated Microcomputer
			-		chnical Q&A
				Tit	le
Doforonce					
References					

Product	Common	Q&A No.		QA300H-134		
Topic	Operating the SCI in External Clock M	ode				
Question When the 1. Does compappli (tran	When the SCI is operated in clock-synchronous external clock mode: 1. Does the SCI start the next transmit operation if, after the completion of 1 byte of data transmission, the external clock is applied to the SCK pin before the H8/300H CPU writes to the TDR (transmit data register)?			Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller		
Answer			-	ITU Watchdog timer SCI A/D converter I/O ports Related Manuals		
	s are as follows:		-	Manual Title		
 Transmission does not start. The next transmission will not start until the TDRE (transmit data register empty) of the SSR (serial status register) is cleared to 0. Reception starts, however, an overrun error will occur unless the RDRF (receive data register full) of the SSR is cleared before the next data is completely received. 			R (serial	Other Technical Documentation Document Name		
				Related Microcomputer Technical Q&A Title		
References	S					

Product	Common	Q&A No.	QA300H-135				
Торіс	System Clocks and SCK Phases						
Question	uestion Classification—H8/300H						
					Software		
Is the SCK (serial transfer clock) output synchronous to system clock (φ)					Registers		
rise or fall?					Bus controller		
					Interrupts		
					Resets		
					Power-down mode		
					Instructions		
					Miscellaneous		
					DMA controller		
					ITU		
					Watchdog timer		
					SCI		
					A/D converter		
					I/O ports		
					70 ports		
Answer				Ra	│ lated Manuals		
Allower					nual Title		
	signal is output synchronous to system	(1)		Otl	her Technical		
					cumentation		
					cument Name		
				Re Tec	lated Microcomputer chnical Q&A		
				Titl	le		
References				1			

Proc	Product Common Q&A No.		QA300H-136					
Topi	С	Changing the A/D Mode and Channel	During A/D (Conversion				
Que	stion				C	Classification—H8/300H		
						Software		
1.	How	do I switch the A/D conversion mode during A/D conversion?				Registers		
2.	Ном	do I change the selected channel during A/D conversion?				Bus controller		
۷.	110 W	do i change the selected channel during	elected chainles during A/D conversion?			Interrupts		
						Resets		
						Power-down mode		
						Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer SCI		
						A/D converter		
						I/O ports		
Ana					D.	lated Manuala		
Ans	swer				Related Manuals Manual Title			
1.	Swite	ching the A/D conversion mode during	A/D conver	rsion will	IVIa	inuai Titie		
decrease conversion accuracy. We advise against it.								
_	C1			a				
2.		ging the selected channel during A/D c						
		problem as switching the conversion n	node. Agam	, we advise		ban Tarbutaat		
	against it.			Other Technical Documentation				
					Do	cument Name		
						lated Microcomputer		
					Tit	chnical Q&A		
					- 110	ie_		
Refe	rences							
		itching the A/D conversion mode or ch		selected channe	el, ch	eck the ADF (A/D end		
flag) in the ADCSR (A/D control/status register).								

Product	Common		Q&A No.	QA300H-137				
Topic	Using General-Purpose Ports							
Question	Classification—H8/300H							
C		.1.4. 1.24. 1	I/O 1.			Software		
Can instructions that manipulate bits be used on I/O ports when a bit of the port is designated an output port?						Registers		
the port is designated an output port:						Bus controller		
						Interrupts		
						Resets		
						Power-down mode		
						Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
					0	I/O ports		
Answer						Related Manuals		
Yes. When a port set as an output port is read by the CPU, the contents of the port data register (DR) are read, regardless of the pin state. When an input port is read, the pin state is read. This means there are no problems in using instructions that manipulate bits. When there are pins in the port that have been designated input ports, however, the DR values of the								
input ports will become undefined (pin state). (See figure 2.27.)						Other Technical Documentation		
		Output Input			Do	cument Name		
	DDR contents Pin status	settings settings 1 1 1 1 0 0 0 0 1 1 0 0 1 1 0 0						
DR contents					Related Microcomputer			
ins	Read DR DR contents after struction BCLR #7, @DR is executed	1 0 1 0 1 1 0 0 Read DR Read pin values values 0 0 1 0 1 1 0 0	Bit 7 set 1 by CP Change pin statu	U s with	Tit	chnical Q&A		
	Figure 2.27 Using General-Purpose Ports							
Defenses		8 - : mp						
References								
The BSET	The BSET, BCLR, BNOT, BST and BIST instructions manipulate bits.							

Product	Common	Q&A No.		QA:	300H-138
Topic	Processing Ports When Not in Use		1		
Question				С	lassification—H8/300H
]				Software
How should I process ports that are not in use?					Registers
					Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					F
Answer				Rel	ated Manuals
1 (1)		(O	4 41	Ma	nual Title
	r the DDR (data direction register) of I/ put state and pull each pin up or down v				
	t 10 k Ω .	with a resisti	ance or		
abou	t 10 K22.				
2. Hand	lle input-only ports the same way.				
					ner Technical cumentation
				Do	cument Name
				Rel	ated Microcomputer
					chnical Q&A
				Titl	е
Reference	s				
	-				